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New Directions in Seismic Hazard Assessment

through Focused Earth Observation

in the Marmara Supersite

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[Long-term monitoring experiment in geologically active regions of Europe prone to natural hazards: the Supersite concept]

D8.4

DESIGN OF THE NEXT GENERATION AUTONOMOUS, MULTI-PARAMETER SEAFLOOR INSTRUMENTATION

TECNICAL REPORT N.2

DIGITIZER AND POWER MANAGEMENT SYSTEMS DETAILS

AUTORS

Marco Zora [a], Alfonso Zaffuto[b], Francesco Italiano[c], Louis Geli[d]

(a) IAMC-CNR U.O.S. di Capo Granitola (TP) - Italy
(b) DAIMAR s.r.l.
(c) INGV Palermo (PA) - Italy
(d) IFREMER - France

Summary

MARSITE PARTNERS

KOERI (Bogazici University, Kandilli Observatory and Earthquake Research Institute)	Turkey
GFZ (Helmholtz-Zentrum Potsdam Deutsches GeoForschungsZentrum)	Germany
TUBITAK (The Scientific & Technological Research Council of Turkey)	Turkey
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IFSTTAR (French Institute of Science and Technology devoted to Transport, Planning and Networks)	France
GURALP Systems Ltd	UK
DAIMAR s.r.l.	Italy
SARMAP s.a.	Switzerland

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Due Date Of Deliverable	30 March 2016

Introduction

Just as described in detail in the report N.1 (**SYSTEM ARCHITECTURE AND PRELIMINARY TESTS**), the whole **underwater** system consist of three main modules: **Power Management System**, **Digitizer**, **Embedded Computer**. In this report, we describe the main features of the modules that have been designed and made by the development team of the CNR and Daimar.

1. Power Management Systems (PMS)

The whole system is electrically powered by the PMS card. The following is the PCB schematic of the PMS card:

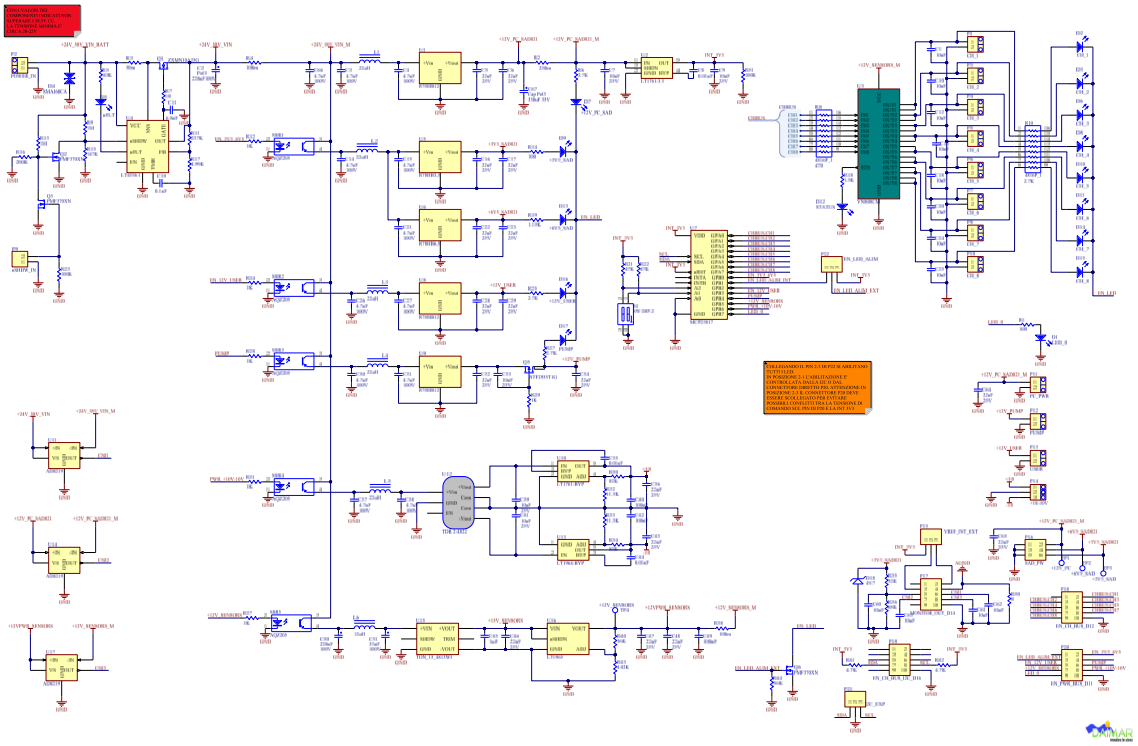


Figure 1: Power Management System (PMS) Schematics

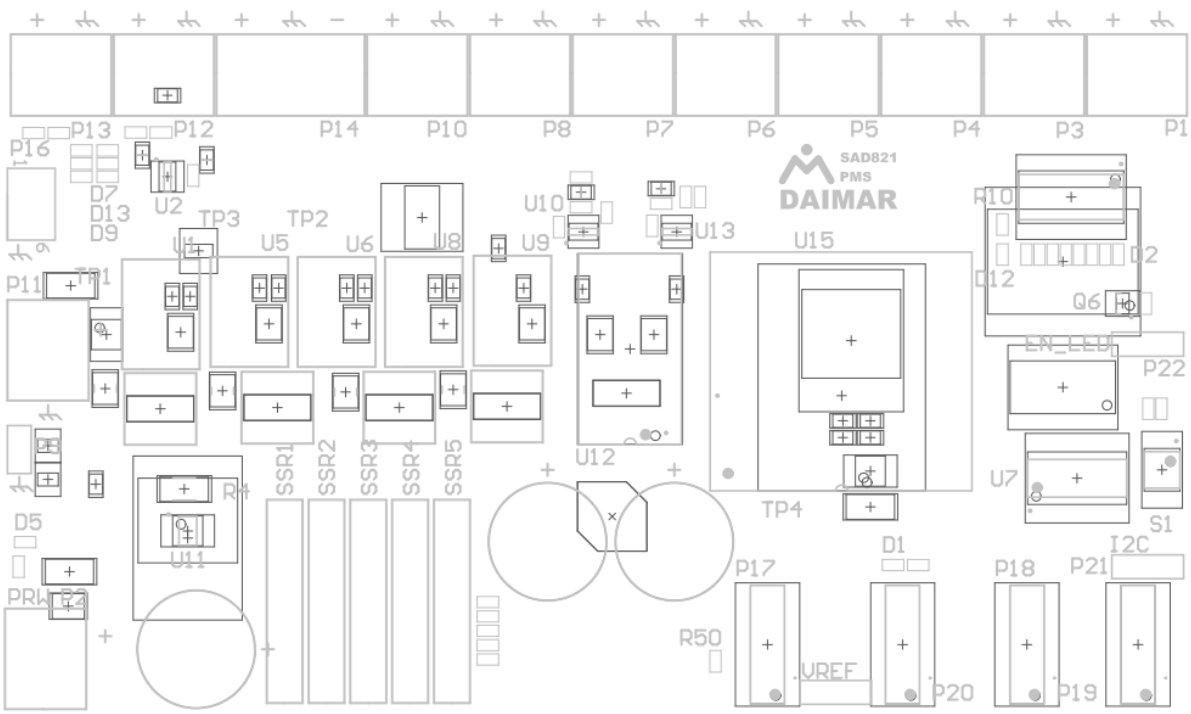
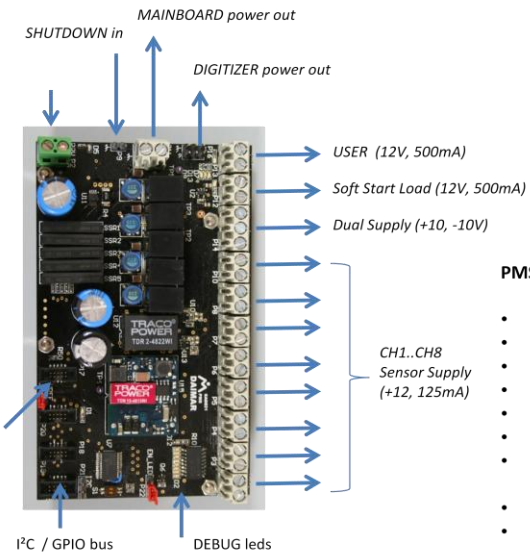
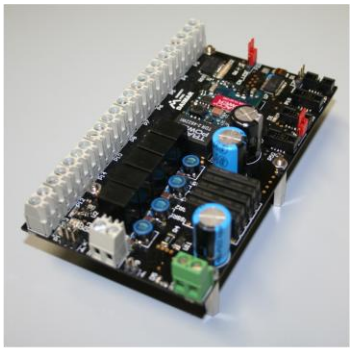


Figure 2: Top Layer of PMS





PMS (Power Management System) MAIN FEATURES

- I²C / GPIO Communication Interface
- Up to FOUR PMS can be connected on the same I²C bus
- Ability to power up to 11 loads with output voltage 12V, ± 10V
- Low Ripple photo-coupled Switching Regulators
- Current consumption monitoring
- DEBUG and LOW POWER mode
- SHUT-DOWN and WAKEUP mode to reduce the energy consumption (MICROWATT MODE)
- HOT-SWAP input protection circuits
- OVER CURRENT and SHORT CIRCUIT protection on all channels outputs
- Supply voltage range from 22V to 60V

Figure 3: PMS rev.1 LAYOUT

1.1 HOT SWAP and multiple switching regulators

The board can be powered from the main supply rail and accept a Vin voltage range from 20V to 58V. The input have a hot swap stage for protection against insertion voltage spike and a maximum 500mA limit current at 58V.

The LT4656 regulates the output during an overvoltage event, such as load dump, by controlling the gate of an external N-channel MOSFET. The output is limited to a safe value thereby allowing the loads to continue functioning.

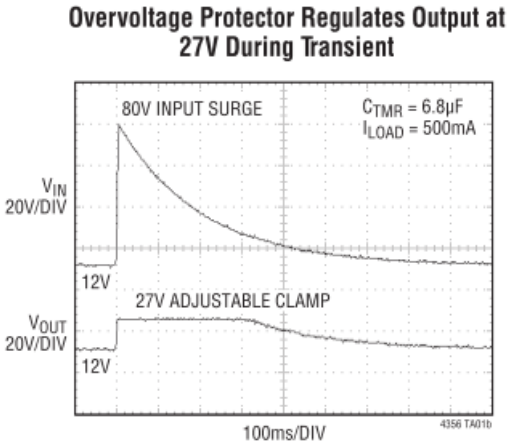


Figure 4: LT4656 Hot Swap specifications

A fault event is indicated by a red led D5 (nFLT). If the condition persists, the MOSFET is turned off. After a cool down period, the GATE pin pulls up turning on the MOSFET again.

Each 12V Sensor output is powered by a RECOM R-78BH DC/DC Converter. The R-78HBxx-Series high efficiency, high input voltage switching regulators are ideally suited to replace 78xx linear regulators and are pin compatible. The efficiency of up to 96% means that very little energy is wasted as heat so there is no need for any heat sinks with their additional space and mounting costs. An input voltage range of up to 8:1 is unsurpassed by any other converter and allows the full stored energy utilization of standard and high voltage batteries. The fully protected output is ideal for industrial applications (especially for industry standard 24VDC bus supplies). Low ripple and noise figures and a short circuit input current of typically only 15mA round off the specifications of this versatile converter series.

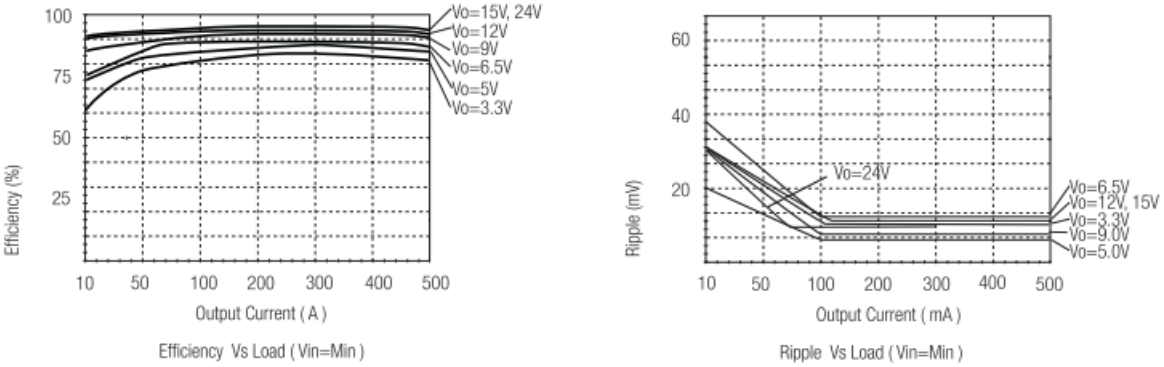


Figure 5: RECOM R-78BH DC/DC converter specifications

1.2 I2C BUS

I²C (Inter-Integrated Circuit), pronounced I-squared-C, is a multi-master, multi-slave, single-ended, serial bus used for attaching low-speed peripherals to computer motherboards and embedded systems.

The board is controlled by the PC with an I2C communication bus (connector P19) and you can turn on and off selectively all utilities. The address can be set with a DIP switches (S1) and you can connect up to four PMS on the same bus. Alternatively you can directly control the board with 3.3V CMOS logic signals from the connectors P18 and P20.

The Microchip MCP23017 device provides 16-bit, general purpose parallel I/O expansion for I2C bus. The 16-bit I/O port functionally consists of two 8-bit ports (PORTA and PORTB). The on-chip POR circuit holds the device in reset until VDD has reached a high enough voltage to deactivate the POR circuit (i.e., release the device from reset). The I2C write operation includes the control byte and register address sequence, as shown in the bottom Figure. This sequence is followed by eight bits of data from the master and an Acknowledge (ACK) from the MCP23017. The operation is ended with a Stop (P) or Restart (SR) condition being generated by the master.

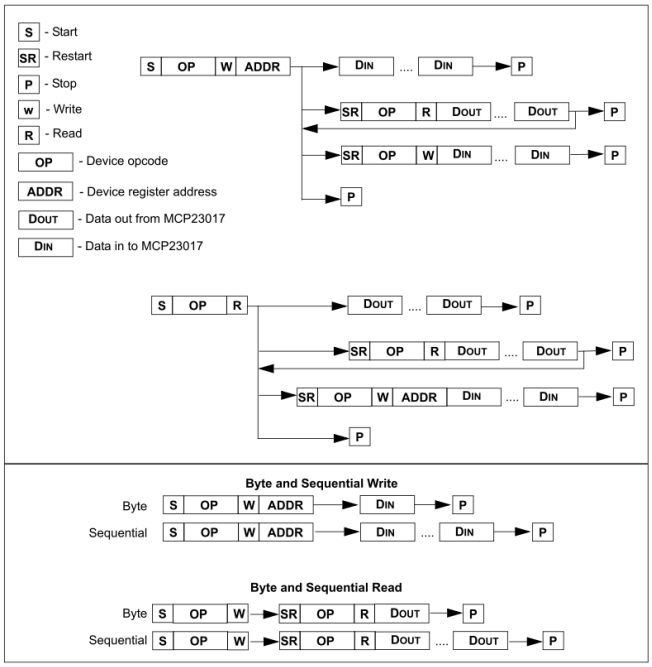


Figure 6: MCP23017 Write/Read format

The output of the 16 bit I/O is connected to two Octal channel high-side driver (ST VN808-E).

The VN808-E is a monolithic device, realized in STMicroelectronics VIPower M0-3 technology, intended to drive any kind of load with one side connected to ground. Active current limitation combined with thermal shutdown and automatic restart, protect the device against overload. In overload conditions, the channel turns OFF and ON again automatically in order to maintain the junction temperature between T_{TSD} and $T_{R.}$ If this condition makes case temperature reach T_{CSD}, overloaded channels are turned OFF and restart only when case temperature decreases down to T_{CR}. Non-overloaded channels continue to operate normally. The device automatically turns OFF in case of ground pin disconnection. This device is especially suitable for industrial applications conform to IEC 61131.

1.3 Analog Current Monitor

The connector P17, provides the voltages for the monitoring of the current consumption values of the system (these voltages are proportional to the currents through appropriate shunt resistors) and can be read directly from the embedded PC.

The outputs to power sensors (CH1-CH8) are protected against short circuits and can provide a maximum current of 700mA 12V on a single channel, or 125mA 12V on all channels simultaneously turned on.

The outputs P12 and P13 can provide 500mA 12V of inductive loads, while the output P14 generates a voltage of + 10V and -10V which is necessary to power particular types of multi-parameter sensors.

2. DAIMAR DIGITIZER (SAD821)

The SAD821 digitizer was developed to get the most in terms of data quality and integration with other embedded systems. Its open architecture allows interfacing with other systems via High-Speed USB or via SPI (Serial Peripheral Interface) low-level protocol.

All internal devices are connected to a single FPGA (**F**ield **P**rogrammable **G**ate **A**rray) that is reprogrammable through a JTAG port (**J**oint **T**est **A**ction **G**roup).

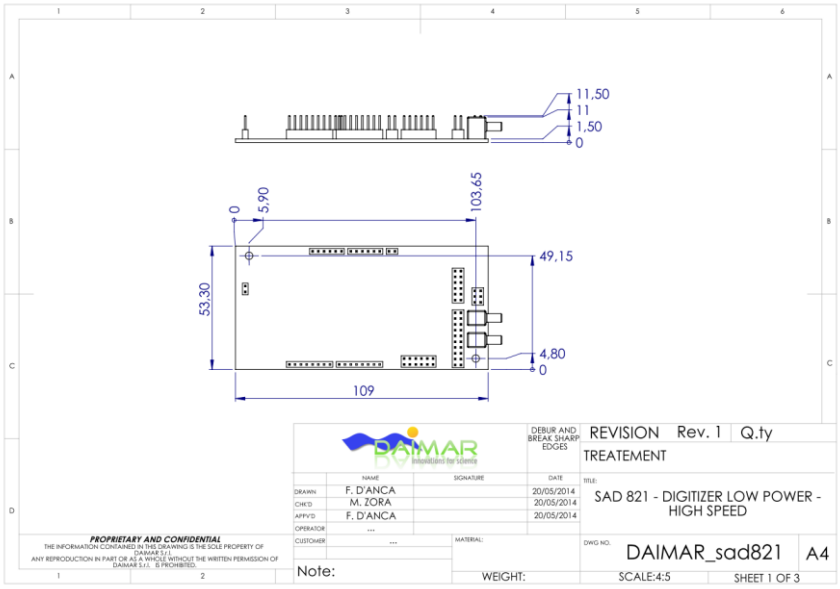


Figure 7: Mechanical layout of the SAD821

2.1 Analog Front End

The SAD821 has 8 analog input channels. The presence of 8 micro-switches (one for each channel) allows you to select one of three types of analog input: voltage, current or direct. In the latter case, the pins of the input signal of the card are connected directly with those of the analog-digital converter bypassing the analog front-end.

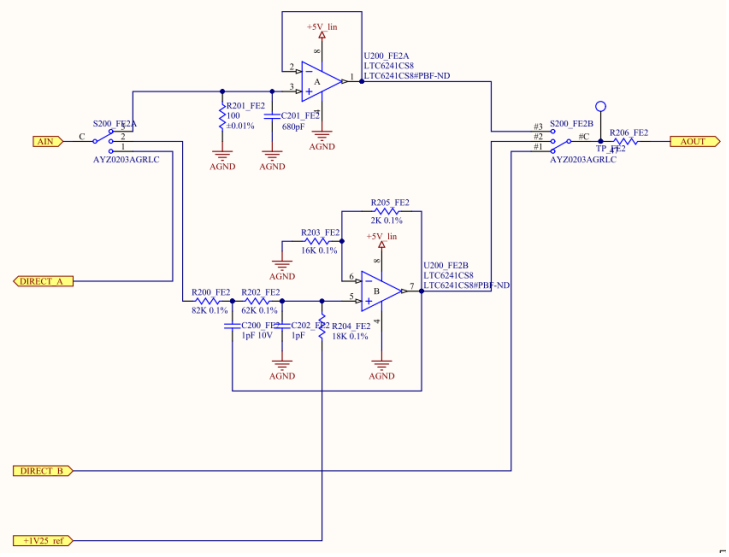


Figure 8: Analog input channel schematic

2.2 Voltage Input

In voltage mode, it converts the analog input voltages between -10V and +10V in a voltage between 0V and 2.5V. The Level shifting and range scaling is realized with an operational amplifier, five resistors suitably sized, two capacitors and a reference voltage of 1.25 V. The low noise operational amplifier is the LTC6241 from Linear Technology. It is a low noise, low offset, rail-to-rail output, unity gain stable CMOS op amps that feature 1pA of input bias current. The 0.1Hz to 10Hz noise of only 550nVP-P, along with an offset of just 125µV are significant improvements over traditional CMOS op amps. Additionally, noise is guaranteed to be less than 10nV/√Hz at 1kHz. An 18MHz gain bandwidth, and 10V/µs slew rate, along with the wide supply range and low input capacitance, make them perfect for use as fast signal processing amplifiers.

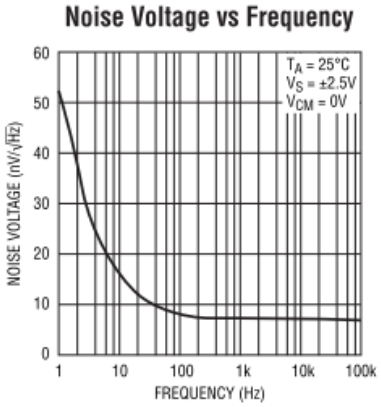


Figure 9: LTC6241 Operational Amplifier specifications

The resistors used, have an accuracy of ± 0.1%. The two capacitors together with the other components, constitute a Sallen-Key filter. The Sallen Key filter is a type of active filter, known and popular due to its simplicity. The circuit behaves as a two poles low pass filter with a bandwidth of 3 MHz.

2.3 Current Input

In current mode, the analog input is able to measure currents between 0 and 25mA. A resistor of 100Ω transforms this current into a voltage between 0 and 2.5V; this is the measuring range of the analog-digital converter. The resistor is connected to a voltage buffer made with an operational amplifier. This buffer decouples the current input from the analog-digital converter, which has an input impedance differential that can reach 14 kΩ.

In parallel to the 100Ω resistor, it is located a capacitor of 680 pF which serves to reduce the bandwidth of the analog stage. As is apparent from the simulations carried out with LTSpice, the bandwidth at 3 dB of the stadium of the current is 3.5 MHz. The 100Ω resistor has a high stability as a function of the temperature (± 5ppm / ^{o}C) and an accuracy of ±0,01%.

2.4 Frequency Input

Frequency measurement is one of the most basic and important method in electronic measurements. Frequency signals are strong anti-interference, easy to transmit, and can be measured with higher precision. The commonly used frequency measurement methods are direct frequency measurement, direct period measurement, ratio-metric measurements and equal precision frequency measurement. The maximum advantage of equal precision frequency measurement method compared to other frequency measurement methods is that it can achieve the equal precision in the entire frequency range, and have nothing to do with the size of the signal frequency.

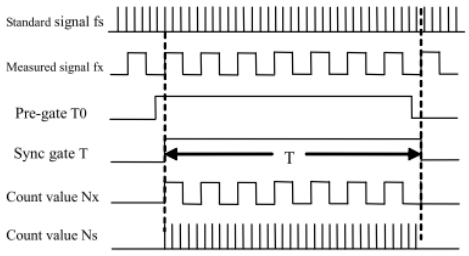


Figure 1. Schematic diagram of equal precision measurement.

ment, we can obtain:

$$T = \frac{N_x}{f_x} = \frac{N_s}{f_s} \quad (1)$$

After deformation, we obtain:

$$f_x = \frac{N_x}{N_s} f_s \quad (2)$$

Differentiating to the above equation, obtain:

$$df_x = \frac{f_s}{N_s} dN_x - \frac{N_x}{N_s^2} f_s dN_s + \frac{N_x}{N_s} df_s \quad (3)$$

For $dN_x = 0$, $dN_s = \pm 1$, and $\frac{N_x}{f_x} = \frac{N_s}{f_s}$

Thus:

$$\frac{df_x}{f_x} = \pm \frac{1}{N_s} + \frac{df_s}{f_s} \quad (4)$$

Figure 10: Equal precision algorithm

The 27 MHz clock in the SAD821 DAIMAR digitizer, is selected as the system clock of this measurements. With this technique, in a second, we can measure a frequency with a relative error of 1/Ns = 3.7 x 10-8. The results show that the relative error is very small and constant in the whole measurement range. At the same time, the design has great flexibility, high integration, with some reference value. Especially in the field of electronic design, where SOC technology has recently become increasingly mature, this design shows great significance.

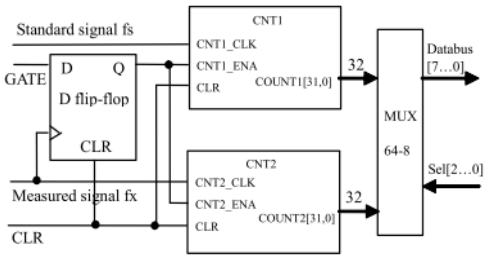


Figure 11: Block digram of equal precision frequency

We tested this algorithm with **SBE 3F CTD Temperature Sensor** with a Temperature accuracy of ± 0.001 ^{o}C. The output signal is a ± 0.5V square wave. Tests have shown that the digital data acquired are not affected by significant errors conversion, thus maintaining unchanged the accuracy of the measurement. Experience has taught us that the sensors that generate a frequency signal, are the

most suitable for a system that wants to maintain a high accuracy with reduced energy consumption than those that generate a voltage or a current signal.

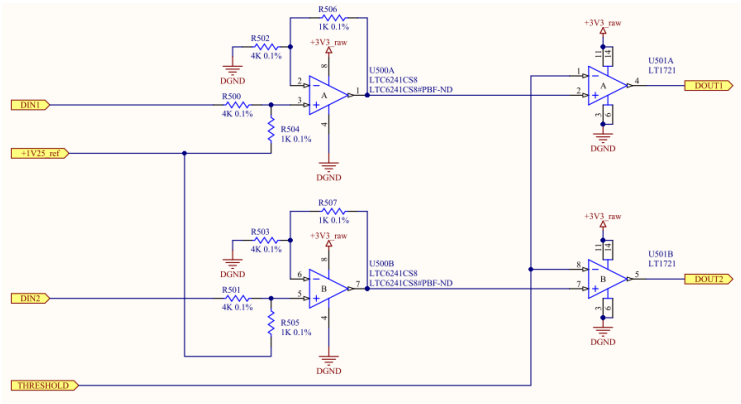


Figure 12: Schematic input front-end for Frequency measurement

In the electronic card SAD821, there are two inputs for digital signals. The digital inputs are connected to a first analog stage that serves as the adapter voltage level. This analog circuit, realized by operational amplifiers, transforms a voltage signal from -1V and + 1V to a voltage signal between 0 V and + 3.3 V.

This voltage signal output from the first stage is compared with a voltage value of the analog reference, set via software. The comparators used are the LT1721 from Linear Technology.

2.5 PASSIVE Hydrophone Input

The hydrophone is a high impedance transducer and the associated signal conditioning circuitry must be carefully designed to meet the challenges of low bias current, low noise, and high gain. The schematic show a configuration with two stage amplifier with total gain of 117 (about 40dB) and 50 kHz bandwidth, plus a dc servo for eliminating leakage currents at the output.

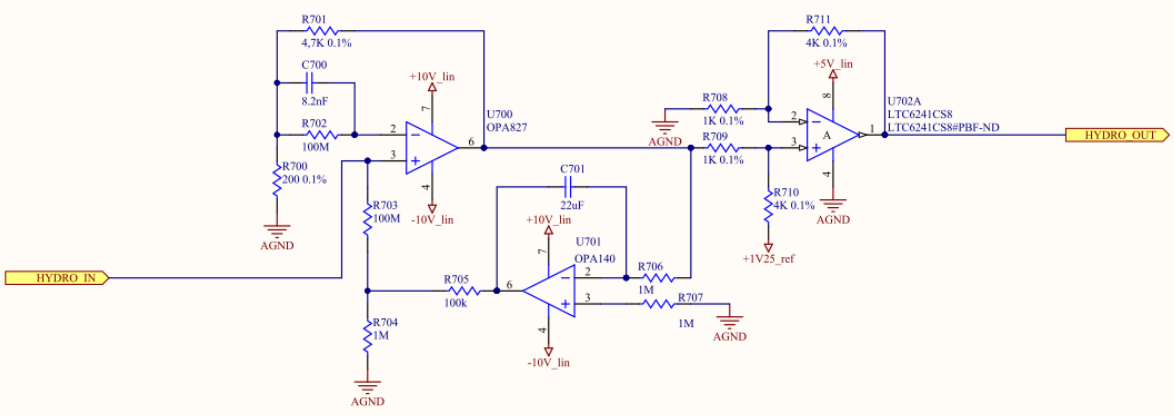


Figure 13: Passive Hydrophone front end schematic

The first stage is a high input impedance low noise amplifier in non inverting configuration with gain of 23.5 and balance input bias current network. The op-amp is an OPA827 JFET operational

amplifiers combine outstanding dc precision with excellent ac 4nV/√Hz at 1kHz performance. These amplifiers offer low offset voltage (150µV, max), very low drift over temperature (0.5µV/°C, typ), low bias current (3pA, typ.), and very low 0.1Hz to 10Hz noise (250nVPP, typ.).

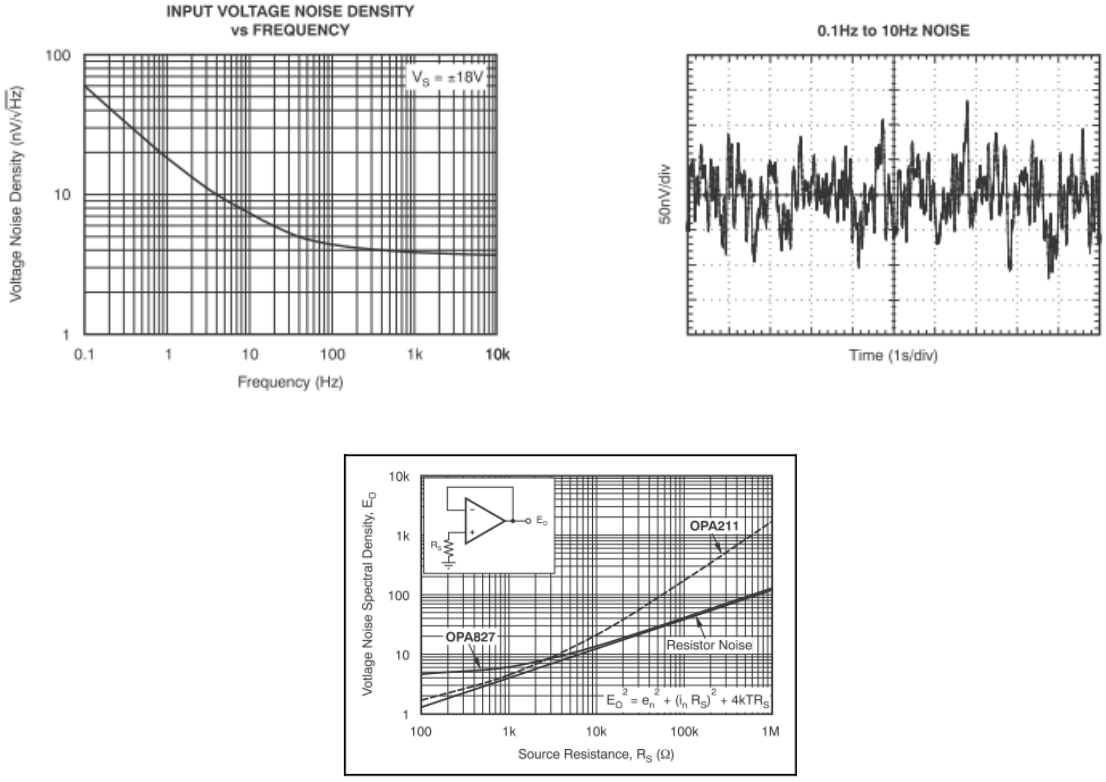


Figure 14: Noise Performance of the OPA827 operational amplifier

DC leakage currents at the output of the hydrophone are subtracted by the servo action of the feedback amplifier. This amplifier need not have the low voltage noise of the OPA827 but can be chosen to minimize the overall system supply current.

The second stage is a non inverting low noise amplifier with gain of 5 add an offset of 1.25V in mid scale of ADC for signal level shifting. The op amp is a LTC6241 low noise CMOS input amplifier.

2.6 ADC

The ADS1278 is 24-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with data rates up to 144k samples per second (SPS), allowing simultaneous sampling of eight channels.

Traditionally, industrial delta-sigma ADCs offering good drift performance use digital filters with large passband droop. As a result, they have limited signal bandwidth and are mostly suited for dc measurements. High-resolution ADCs in audio applications offer larger usable bandwidths, but the offset and drift specifications are significantly weaker than respective industrial counterparts. The ADS1278 combine these types of converters, allowing high-precision industrial measurement with excellent dc and ac specifications.

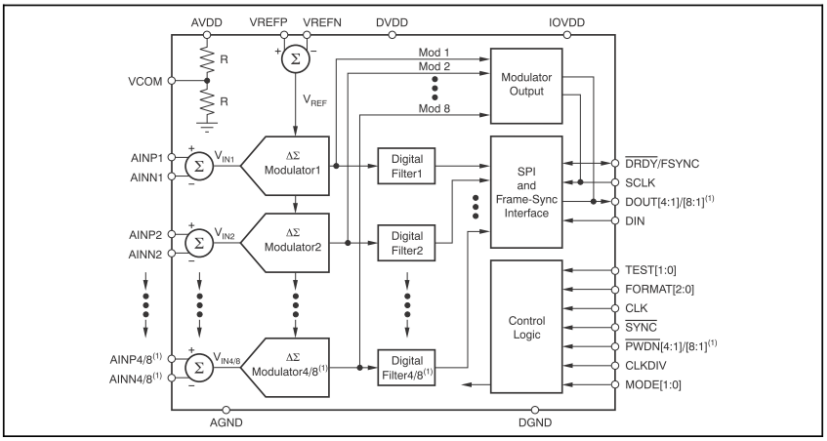


Figure 15: diagram of ADS1278 Analog to Digital Converter

The converter is composed of two main functional blocks to perform the ADC conversions: the modulator and the digital filter. The modulator samples the input signal together with sampling the reference voltage to produce a 1s density output stream. The density of the output stream is proportional to the analog input level relative to the reference voltage. The pulse stream is filtered by the internal digital filter where the output conversion result is produced. In operation, the input signal is sampled by the modulator at a high rate (typically 64x higher than the final output data rate). The quantization noise of the modulator is moved to a higher frequency range where the internal digital filter removes it. Oversampling results in very low levels of noise within the signal passband. Since the input signal is sampled at a very high rate, input signal aliasing does not occur until the input signal frequency is at the modulator sampling rate. This architecture greatly relaxes the requirement of external antialiasing filters because of the high modulator sampling rate.

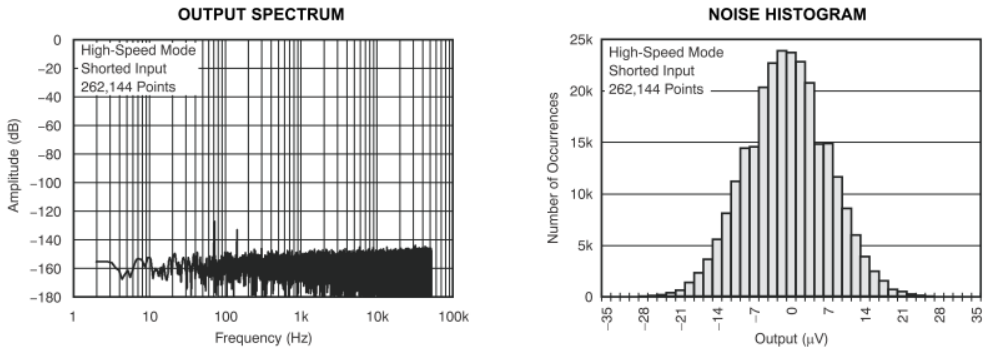


Figure 16: ADS1278 Noise performances

The SPI-compatible format is a read-only interface. The SPI format is limited to a CLK input frequency of 27 MHz.

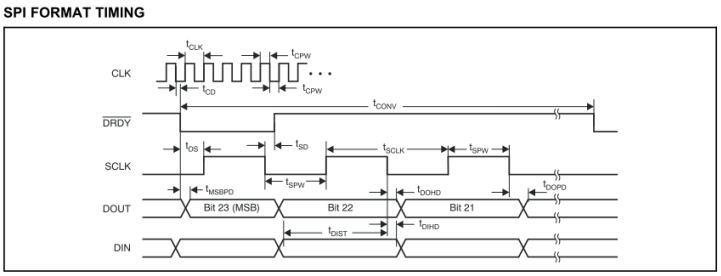


Figure 17: ADS1278 serial communication bus

Table 1: Operating Mode Performance Summary of ADS1278

MODE	MAX DATA RATE (SPS)	PASSBAND (kHz)	SNR (dB)	NOISE (μV_{RMS})	POWER/CHANNEL (mW)
High-Speed	144,531	65,472	106	8.5	70(1)
High-Resolution	52,734	23,889	110	5.5	64
Low-Power	52,734	23,889	106	8.5	31
Low-Speed	10,547	4,798	107	8.0	7

(1) Specified at 105kSPS.

The channels of the ADS1278 can be independently powered down by use of the PWDN inputs. When channels are powered down, the ADS1278 enters a microwatt power state.

The data coming from the AD converter, are stored in a Static Random Access Memory (SRAM). This memory serves as a buffer between the digitizer and the external computer so as to ensure the real-time operation. The chip used is a Cypress CY62177EV30 MoBL 4M x 8 bit SRAM.

The CY62177EV30 is a high performance CMOS static RAM organized as 4 M words by 8 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®). The device also has an automatic power down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. Following are the main features :

- Very high speed – 55 ns
- Wide voltage range – 2.2 V to 3.7 V
- Ultra low standby power – Typical standby current: 3 µA / Maximum standby current: 25 µA
- Ultra low active power – Typical active current: 4.5 mA at f = 1 MHz

2.7 Digital I/O

All hardware devices are connected to a single FPGA chip. A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (Circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). As FPGA designs employ very fast I/Os and bidirectional data buses it becomes a challenge to verify correct timing of valid data within setup time and hold time. Floor planning enables resources allocation within FPGA to meet these time constraints. FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of a portion of the design and the low non-

recurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost), offer advantages for many applications.

The chip used in the SAD821 digitizer is a LATTICE MachXO2. The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I2C controller and timer/counter. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption.

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system.

Table 2: FPGA Power Saving Features

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

The NETBUS is accessible from a standard *Arduino* type connector. In this mode, the SAD821 can becomes a SHIELD for Arduino. Communication, between the external microcontroller and the digitizer, is via SPI protocol.

The digitizer is equipped with an expansion socket compatible with the DLP-USB1232H module. The DLP-USB1232H is DLP Design's premier USB-to-UART/FIFO interface module based on FTDI's 5th generation USB 2.0 High Speed (480Mb/s) silicon. With a special FPGA firmware, you can create a USB to parallel FIFO transfer data rate up to 8 Mbyte/Sec. The function of the I/O pins is determined by the configuration that is stored in the EEPROM connected to the FT2232H USB IC. The following table details the function of each pin for the specified mode:

Table 3: FT2232H USB module interface with SAD821 FPGA

DLP-USB1232H							
Pin		Pin Functions For Each Supported Mode					
Pin #	Pin Name	ASYNC Serial (RS232)	245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	CPU Target
Channel A							
18	ADBUS0	TXD	D0	D0	D0	TCK/SK	D0
16	ADBUS1	RXD	D1	D1	D1	TDI/DO	D1
2	ADBUS2	RTS#	D2	D2	D2	TDO/DI	D2
5	ADBUS3	CTS#	D3	D3	D3	TMS/CS	D3
17	ADBUS4	DTR#	D4	D4	D4	GPIOL0	D4
4	ADBUS5	DSR#	D5	D5	D5	GPIOL1	D5
13	ADBUS6	DCD#	D6	D6	D6	GPIOL2	D6
3	ADBUS7	RI#	D7	D7	D7	GPIOL3	D7
15	ACBUS0	TXDEN	RXF#	**	**	GPIOH0	CS#
14	ACBUS1		TXE#	WRSTB#	WRSTB#	GPIOH1	A0
11	ACBUS2		RD#	RDSTB#	RDSTB#	GPIOH2	RD#
12	ACBUS3	TXLED#	WR#	**	**	GPIOH3	WR#
7	ACBUS4	RXLED#	SIWUA	SIWUA	SIWUA	GPIOH4	SIWUA

3. Mechanical Layout

We started to explore new solutions in the design of mechanical vessel for harsh marine environments and deep sea. The alloys of interest to us are:

- INCONEL
- MONEL
- TITANIUM
- Stainless Steel AISI 304-316
- Aluminium AW6063 with hard anodizing
- The plastics interesting for these applications are:
- Nylon
- Polyethylene
- PVC
- PEEK
- Kapton
- Mylar

INCONEL® alloy 625 is an excellent choice for sea-water applications, as it is resistant to pitting and crevice corrosion and has high corrosion-fatigue strength, high tensile strength, and is resistant to chloride-ion stress-corrosion cracking. Used in wire rope, propeller blades, propulsion motors and sheathing for undersea communication cables, this versatile alloy has earned its place in the marine industry. Down-hole equipment, like hangers, uses another super alloy, INCOLOY® alloy 718 for its high strength and corrosion resistance.

Figure 1: DAIMAR module, tested up to 2000m depth on URANIA-CNR oceanographic ship

MONEL® alloy 400 is a nickel-copper alloy that is stronger than pure nickel and can be fabricated readily by hot- and cold-working, machining, and welding. MONEL alloys are resistant to corrosion by many agents, including rapidly flowing seawater. This feature, coupled with its resistance to bio-fouling and microbially induced corrosion (MIC), makes MONEL a cost-effective and robust alloy for the manufacture of wave protection sheathing for platform risers and steel pylon legs on offshore rigs.