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Perspectives and advantages of the use of excimer laser annealing for MOS technology

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Summary. — The integration of excimer laser annealing (ELA) into the MOS device technology has been studied and evaluated within the frame of the IST project FLASH (Fundamentals and applications of laser processing for highly innovative MOS technology), funded by the European Commission. The final aim of the project was to demonstrate that ELA can be applied as a reliable, effective and advantageous process in the context of semiconductor device fabrication. Some of the results of this activity are summarised, relative to the experimental characterization and theoretical modelling. The electrical characterization of the transistor fabricated by ELA is also presented, showing a device yield of 90% on wafer.

PACS 61.80.Ba – Ultraviolet, visible, and infrared radiation effects (including laser radiation).
PACS 61.72.Tt – Doping and impurity implantation in germanium and silicon.
PACS 85.30.Tv – Field effect devices.
PACS 85.30.De – Semiconductor-device characterization, design, and modeling.

1. – Introduction and state of the art

Scaling the CMOS technology node below 90 nm will require source/drain (S/D) junction depths shallower than 50 nm [1], as illustrated in fig. 1, the latter extracted from the International Technology Roadmap for Semiconductors 2003. Ultra-shallow, electrically active layers can be formed in Si through a combined process of ultralow energy ion implantation and high ramp rate (400 °C/s), short time (< 1 s), high temperature (> 1000 °C), "spike" annealing [2]. Although the ions are implanted at low energy and their range is very shallow, high temperature annealing is required in order to activate a sufficient fraction of the implanted dopant. On the other hand, non-equilibrium diffusion can lead to increased diffusivity during post-implantation annealing (transient

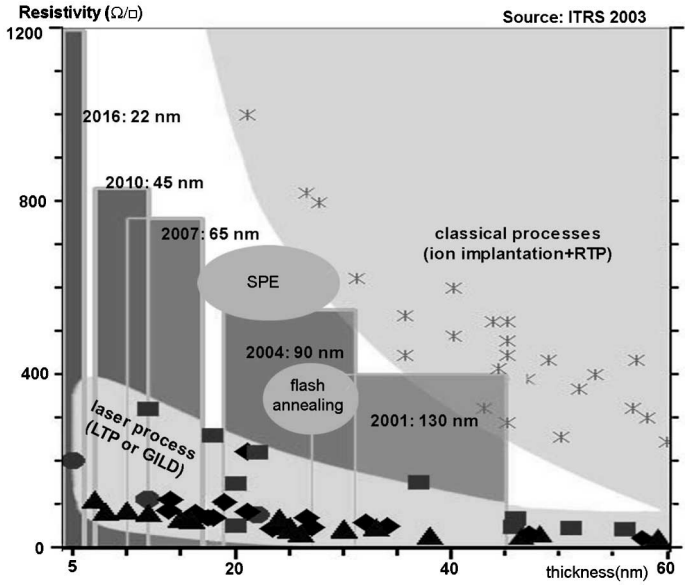

Fig. 1. – Junction depth and sheet resistance requirements according to the ITRS 2003 for the CMOS technology nodes.

enhanced diffusion, TED) [3], seriously limiting the minimum junction depth. Excimer laser annealing (ELA) of ion implanted Si [4, 5] has recently attracted renewed interest within the semiconductor community for its possible application to the formation of ultra-shallow junctions in Si [6-9]. The technique offers many advantages compared to conventional rapid thermal anneal (RTA) procedures, such as control over the junction depth and higher dopant activation efficiency. In fact, when irradiating Si by laser light with sufficient energy density, a well-defined melted zone, with a sharp transition from liquid to crystal phase, is formed. The diffusivity of dopants is raised in the liquid state ($\sim 2 \times 10^{-4}\,\mathrm{cm}^2/\mathrm{s}$ [4]), and the dopants are able to redistribute uniformly within the melted layer giving rise to box like profiles after re-growth. Due to the steep thermal gradient between the liquid and the solid phases, immediately after irradiation the liquid-crystal interface advances towards the surface at a rate of $\sim 5\,\mathrm{m/s}$ [6]. As a result of such rapid solidification (low temperature solid phase regrowth is typically $1.5 \times 10^{-10}\,\mathrm{m/s}$ at $550\,^\circ\mathrm{C}$), less dopant is segregated into the liquid phase at the liquid-crystal interface and enhanced dopant trapping occurs. The fraction of the implant dose which is retained within the semiconductor during ELA is governed by segregation (during re-growth), evaporation (during the melted phase) and ablation (during energy deposition). The electrical activation of the retained dopant in the re-grown layer following ELA is eventually limited by morphological instability at the liquid-crystal interface during re-growth, lattice strain and the thermodynamic limit [10].

Based on these premises, an effort has been produced worldwide during the last few years for making ELA a reliable process to be used in the CMOS technology. The application of ELA to MOSFET devices has been studied and evaluated within the frame of the project FLASH (Fundamentals and applications of laser processing for highly innovative MOS technology) [11], concluded in January 2006, funded by the European

Commission. The goal of the FLASH project was represented by the integration of ELA in the MOS technology. Downscaling such devices is facing a bottleneck; in order to achieve low-resistivity and shallow source regions, dopants are implanted with very high dose, inducing amorphization of the implanted regions. Dopant activation, as well as full recovery of the ion-implantation induced damage, requires high temperatures RTA, with a consequent substantial dopant diffusion, which severely limits the body-drain leakage current as well as the minimum channel length achievable. ELA can perfectly solve these problems, as it allows efficient dopant activation and damage removal, through the melt-regrowth process, while still controlling the junction depth to values well below 100 nm [6-9]. However, as ELA has to be performed with the gate stack already defined, a major issue is related to the undesired effects of laser irradiation of the gate regions.

The major obstacle to tackle, for exploiting the advantages of ELA offered to the CMOS technology, concerns its device integration; the current state of the art in the field of advanced thermal processing for semiconductor devices is rather complex, including several proposals of laser or lamp based methods. However, most of the groups active in this field agree on the significant technological impact that the use of ELA would have in the semiconductor industry. At the Workshop "Non conventional thermal processes for advanced CMOS", held in Roma in 2005, the delegate of Nanyang University (Singapore) pointed out the need for Laser Thermal Processing (LTP) for the next technology nodes, indicating also a possible use of LTP in the sub-melt regime, as a thermal process able to limit the dopant diffusion to a negligible quantity. Quite interesting was the point of view on the development of microprocessors of a world leading company, AMD, that attributed the improvement of the V_{Tsat} roll-off in the AMD transistors to the use of low-energy halo implants, giving less importance to the source/drain extension junction depth and to its abruptness. Although two of the main characteristics of the ELA process were hence claimed to be not so crucial (junction depth, abruptness), the same AMD representative expressed, however, the need for en efficient diffusion-less activation annealing, presently provided by the Flash Lamp Annealing (FLA) and Laser Thermal Processing (LTP) methods. The group formed by the Institute of Fundamental Electronics (IEF), Sopra and other French institutions investigated the use of LTP and Gas Immersion Laser Doping (GILD), concluding that Laser doping, intended either as LTP or GILD, is necessary for the junctions requested by the future technology nodes.

That RTA is surpassed, is also the general message launched by the 13th IEEE International Conference on Advanced Thermal Processing of Semiconductors (RTP 2005), held in USA in 2005. It was pointed out that, while keeping paced with Moore's Law has been so far accomplished by decreasing processing times, fundamental limits are now projected for the 45 nm node, which requires processing time significantly shorter than those available by RTP, on the order of 10 ms or even less and with nearly zero diffusion. This is beyond the processing regime currently provided by lamp based RTP systems, which are instead limited to processing time on the order of 1 s. In order to meet this new processing requirement, big semiconductor industry suppliers, such as Applied Materials, have identified Laser Annealing as one of the process solutions to enable ultra shallow junction formation for the 45 nm technology node. Further signals of interest are represented by the rich production of patents on laser processing for device applications, with several examples reported in 2005.

In this work we discuss some of the results obtained by the FLASH project, including one and two-dimensional analysis of dopant distributions obtained by ELA, process modelling and electrical characterization of the fabricated power MOS devices.

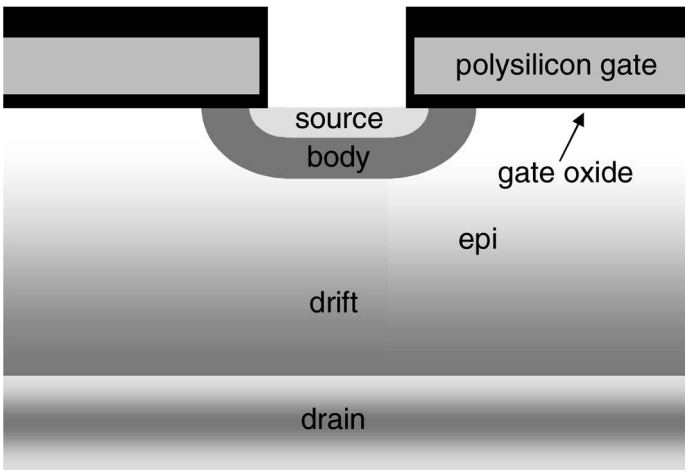

Fig. 2. – Schematic of the MOS structure used for the experiments.

2. – Experimental results

In fig. 2, a schematic of the MOS structure used in our experiments is shown. The source regions are implanted with As and laser annealing is applied to activate the doped regions. In order to improve coupling of the laser radiation with the source regions, 50 nm thick oxide was deposited, such that the reflectivity at 308 nm of the source region was reduced to 34% by the antireflective action of the oxide layer [8]. The same oxide layer also covers the gate stack side walls, thus protecting the structure from mechanical deformations related to melting of the polysilicon gate. A total oxide thickness of 200 nm is instead present on top of the polysilicon gate, not altering the polysilicon gate reflectance ($R = 62\%$) [8]. A cross-section Transmission Electron Microscopy (TEM) micrograph of the structure prior irradiation is shown in fig. 3. The amorphous layer generated by the As implant is visible in the silicon region in between the polycrystalline silicon stripes.

The laser apparatus used for irradiation is a Lambda Physik LPX 205 XeCl excimer laser (308 nm emitted wavelength, 30 ns pulse duration), delivering an homogeneous beam, with a variable spot size, that for our experiments was adapted to the

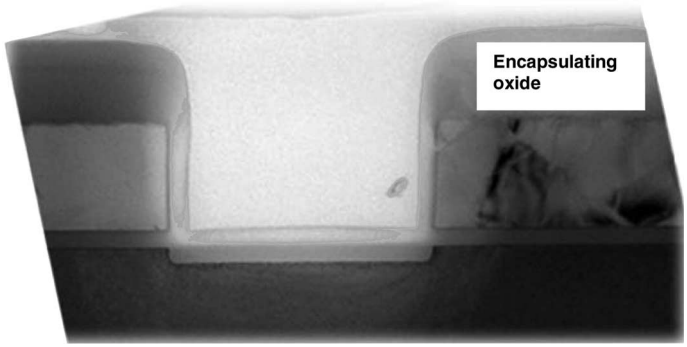

Fig. 3. – Cross-sectional TEM of the fabricated structure.

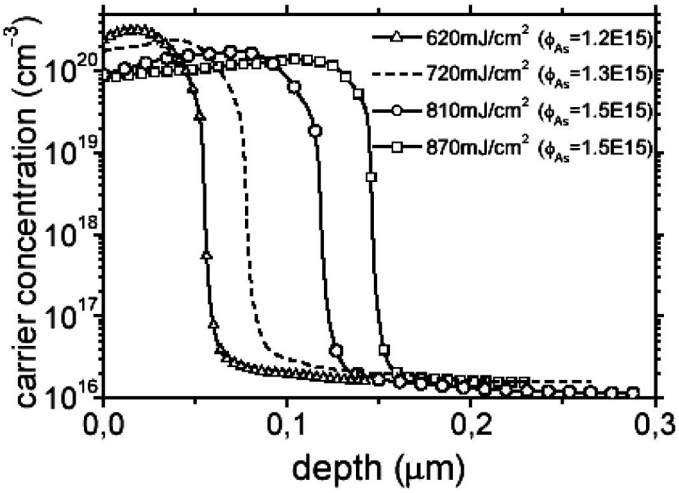

Fig. 4. – Carrier profiles, measured by SRP, after ELA at different energies of a 30 keV As implant. The active dose is reported in the label.

chip size ($2.5 \times 3.5\,\mathrm{mm}^2$), and with an energy density (E_d) that can be continuously changed, by using a beam attenuator, in the range 100–1200 $\mathrm{mJ/cm}^2$. The samples were irradiated in vacuum with a substrate temperature of 500 °C. The possibility to heat the substrate during laser irradiation allows to reduce the threshold energy density for melting (for instance, for $T = 750\,\mathrm{K}$ the threshold energy is $0.5\,\mathrm{J/cm}^2$ while at RT is around $0.8\,\mathrm{J/cm}^2$) and also to increase the melt duration and reduce the re-solidification velocity, thus modifying the incorporation of dopants during re-solidification.

The carrier profiles as a function of depth, as obtained by Spreading Resistance Profiling, associated to the As doping, are reported in fig. 4 as a function of laser energy density; they show a box-like shape with a very high abruptness of 2.6 nm/dec. Due to the extremely high diffusivity of dopants in liquid Si, the As atoms are able to redistribute almost uniformly within the melted layer, up to the interface between the solid and liquid Si. The following rapid re-crystallisation from the liquid phase enhances dopant trapping and produces high electrical activation. The highest carrier concentration is achieved following shallow melting ($620\,\mathrm{mJ/cm}^2$) and decreases as the dopant progressively redistributes deeper into the bulk for higher laser irradiation. Simultaneously, activation improves from $1.2 \times 10^{15}/\mathrm{cm}^2$ to $1.5 \times 10^{15}/\mathrm{cm}^2$ and the sheet resistance decreases from 75 to 49 Ω. Due to lateral heat dissipation occurring in the structured wafers, the junction depths obtained in such non-patterned wafers can be rather different from the real device case. However, the one-dimensional analysis of doping obtained by laser annealing is useful to determine the shape of the dopant profiles and their evolution with the irradiation conditions.

While annealing the source layer, the remaining part of the doped layers composing the MOSFET, such as the boron-doped body, is not altered at all by the laser irradiation. This is due to the short duration of the process, of the order of tens of nanoseconds, as well as by the fast dissipation of the heat through the Si substrate, determining a thermal process in solid phase of the underlying doped layers lasting a few milliseconds, inducing a negligible diffusion not detectable by the analytical techniques.

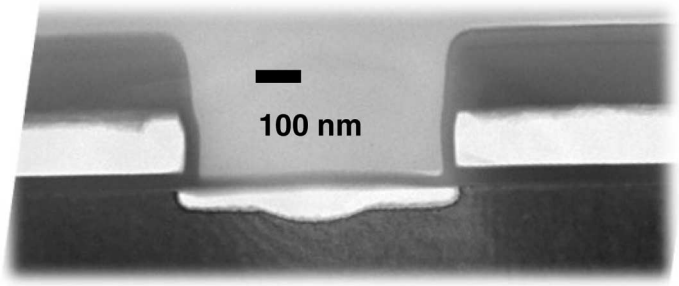

Fig. 5. – MOSFET cross-sections observed by TEM. Selective chemical etch exhibits the source (white region) region obtained by ELA of a 10 keV As implant.

In order to preserve the gate integrity from the morphologic modifications induced by the laser irradiation process, as above illustrated, an oxide layer surrounding the polycrystalline silicon gate electrode was employed. The integrity of the complete device structure after laser irradiation was carefully controlled by Scanning Electron Microscopy, that provides the analysis over a large scale and, in this case, turns out to be a more severe test than Transmission Electron Microscopy, which indeed guarantees a higher resolution, but is limited to a smaller area. The cross-section TEM analysis is very useful, however, when the two-dimensional contour line of the doped region has to be measured, in combination with chemical selective etch thinning of the doped region. An example is reported in fig. 5 after ELA of a 10 keV As implant, where a junction shallower than 100 nm is shown (the corresponding doped region is identified by the white area in the implanted window); a deeper melting occurs in the central region of the implanted window, due to lateral heat loss and to the diffraction of the laser light through the narrow geometries of the patterned sample. The lateral diffusion underneath the gate oxide is negligible, so providing the possibility to shrink the channel length without incurring in short channel effects.

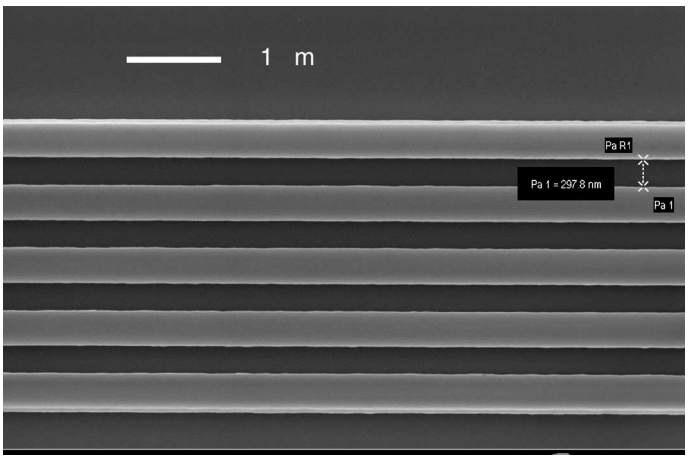

Fig. 6. – Plan view obtained by SEM of a MOSFET structure optimised to be irradiated by laser.

The realization of a device implies the reliability of processing and patterning over a large scale, in order to ensure a high yield, necessary for a real industrialization of the method under investigation. A SEM image of a MOSFET chip irradiated by laser is shown in fig. 6, attesting the integrity of the structure subjected to ELA when operating in optimised conditions.

3. – Two-dimensional numerical modeling

A phase field methodology was preferred to conventional methods for the dopant evolution during melting [12]. Standard modelling is based on the numerical solution of the heat diffusion and on a step-like change of the mass transport properties across the solid/liquid interface, while an *ad hoc* segregation model rules the gap in density across the interface itself. In this sharp interface model, the thermal and mass transport are de-coupled and the segregation coefficient at the interface can be included by fitting the experimental results. For the numerical calculations an obvious drawback of this methodology is that the instantaneous interface position and speed should be found. This poses some limitations, especially for its application in 2D calculations or when the whole device structure has to be considered.

The phase-field methodology is instead based on a physical description of the moving phase boundary problem considering a finite dimension of the transition region between the two phases. Tracking the boundary location is not necessary for the numerical simulations since phase, temperature and dopant density evolve concurrently according to the three coupled differential equations:

$$\frac{\partial \Phi}{\partial t} = -(\mu/6l)\frac{\delta F}{\delta \Phi} = (\mu/6l)\left[\varepsilon^2 \nabla^2 \Phi - \frac{\partial f}{\partial \Phi}\right],$$

$$\frac{\partial c}{\partial t} = \vec{\nabla}\left[(v_m D(\Phi)/RT)c(1-c)\vec{\nabla}\frac{\partial f}{\partial c}\right],$$

$$\rho c_V \frac{\partial T}{\partial t} + 6\Phi(1-\Phi)\big[(1-c)L_{Si} + cL_X\big]\frac{\partial \Phi}{\partial t} = \vec{\nabla}\big[K(\Phi)\vec{\nabla}T\big] + S_{\text{laser}}(r,t),$$

where Φ is the phase, F the free energy, f the potential term, C the dopant concentration, T the temperature and S the light source intensity.

The phase field method, based on the Ginsberg-Landau approach to the phase transition problem, was then applied to the simulation of thermal field evolution and dopant redistribution during ELA of implanted samples.

The requirements of an efficient simulation imposed structural changes in the code for two-dimensional structures [13], such as the space discrete approximation and the method for time integration. In addition, the heat source was numerically evaluated, simulating the interaction between the laser electromagnetic wave and the patterned surface of the Si wafer, by means of the finite difference time domain (FDTD) approach [14]. The FDTD method is based on the numerical solution of the Maxwell equations and we used a square grid with 4 nm spacing and an explicit scheme for the time integration [14].

Such modeling approach allows to quantify the dependence of the junction depth on the position in the implanted window. Figure 7 illustrates a simulated dopant distribution, referring to the case of fig. 4. The blue colour represents melting, that in turn means homogeneously redistributed As. All the main features of the resulting doping distribution after ELA are perfectly reproduced by the model, with a deeper doping profile

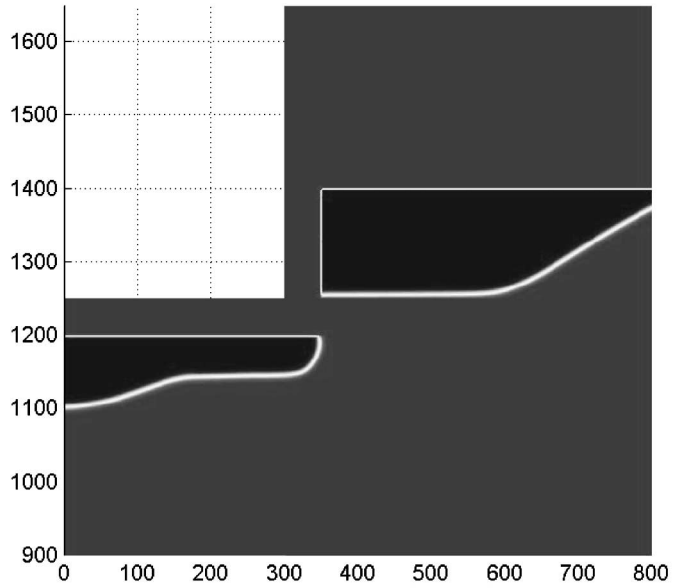

Fig. 7. – Two-dimensional simulation of melting following laser irradiation, as obtained by the phase field calculation.

in the center of the window, resulting from the combined effects of lateral heat diffusion and diffraction effects. This simulation code not only allowed a precise interpretation of the experimental results but also enabled the predictive analysis of different gate stack architectures and geometries and the optimization the ELA conditions.

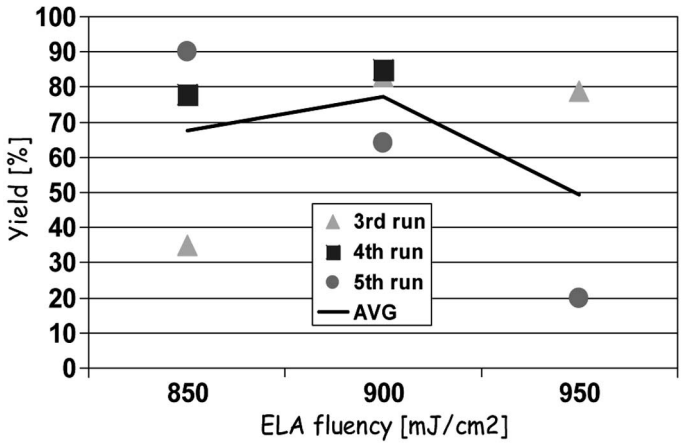

Fig. 8. – MOSFET yield *vs.* ELA energy density.

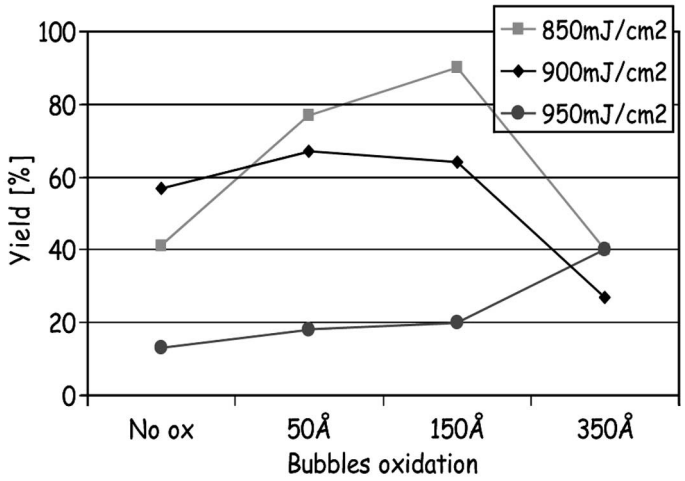

Fig. 9. – MOSFET yield *vs.* oxidation thickness of evental fractures in the encapsulating oxide, cased by melting of the polycrystalline silicon gate electrode.

4. – Integration in MOS technology: Fabrication of transistors

MOS devices have been fabricated according to the structure described in fig. 3; a process flow chart sequence was defined according to the indications from the experiments and the modelling and simulation work. In particular, a careful modulation of the dielectric thickness present on top of the device structure was accomplished, such that an antireflective effect is induced in the implanted window and maximum reflection is generated by the gate stack. The laser annealing process has been realized by a mask projection tool in order to irradiate a single device with a uniform laser beam, avoiding beam tails. The MOSFET yield *vs.* ELA fluency, for the transistors with optimized structure and treated with the most reliable processes, is reported in fig. 8 for three lots of wafers. Both at 850 and 950 $\mathrm{mJ/cm^2}$ a large yield spread is observed for the three lots, whereas the 900 $\mathrm{mJ/cm^2}$ group is more stable with an average yield of about 77%. The spread is due to the non-proper processing, as the wafers traveled from one site to another, geographically distinct, because of the spirit of a European project, exploiting the resources of several partners. Many dust particles can affect the device yield of these wafers, however, surprisingly high yield is still obtained, attesting the robustness of the process.

Since the possibility that a fracture in the surrounding oxide might occur, hence inducing a liquid polycrystalline silicon outflow through the aperture of the broken oxide, an oxidation process has been added after ELA, in order to safely isolate the polycrystalline silicon gate from the source metal. However, the thicker is the grown oxide, the smaller will be the contact openings. This means that the source metal (Al) will be not able to fill the contacts and then the MOS ON parameters will be not good. The maximum yield for all fluencies, with respect to the oxide thickness values, is found ranging from 50 to 150 Å, as shown in fig. 9.

Based on the evaluation of the best yield, as well as on the previously illustrated process refinements, ELA-MOSFETs were fabricated, whose main characteristics are reported in fig. 10. The ELA processed devices have a threshold voltage comparable with

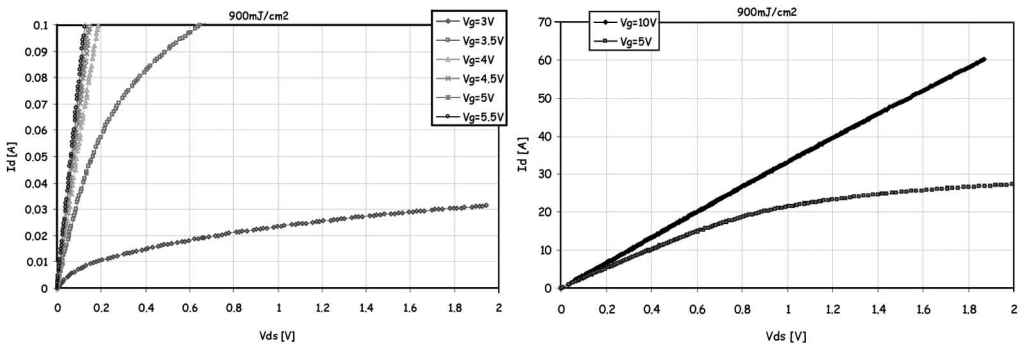

Fig. 10. – ON state characteristics for low (left side) and high (right panel) current.

the conventionally processed device and, if driven at 10 V, the MOSFETs are completely switched on and the ON resistance is comparable with the standard one. Such transistors were fabricated with a yield of $\sim 80\%$.

The reliability of the process was therefore demonstrated; the final aim was to prove that even better electrical performances could be achieved by means of the ELA process. In particular, the peculiarity of the ELA process as a "zero lateral diffusion" thermal treatment was worth exploiting. In order to do that, a lot of MOSFET wafers was prepared, with a shallower body layer and a shorter channel, aiming to a lower ON resistance. The "on" characteristics are shown in fig. 11 for the $900\,\mathrm{mJ/cm^2}$ case. Thanks to the reduction of the channel length, made possible by the use of ELA, that ensures zero lateral diffusion, a 10% decrease of the ON resistance of the transistor was obtained. This is a clear advantage of using ELA, revealing itself as a suitable process to scale the channel length.

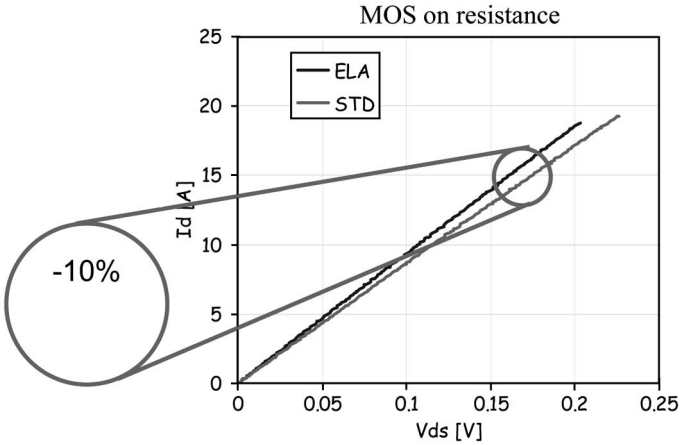

Fig. 11. – Drain current increase for the ELA treated MOSFET, with respect to the device processed by conventional thermal processing.

5. – Conclusions

In this work we reported the recent results obtained within the European project FLASH, aiming to the integration of ELA in the MOSFET fabrication process. The formation of n+/p source junctions has been investigated in both one and two dimensions and a route for the ELA integration is presented. The experimental results have been analysed by using a two-dimensional simulation program, specifically developed. The simulation tool allowed a deeper insight of the ELA process and has been successfully used to optimise the process parameters. Test devices have been fabricated and integrity tests show that a yield of $\sim 80\%$ can be achieved with this process. The present results clearly show that ELA can be successfully integrated in the MOS technology and that extension to other device technologies could be possible.

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REFERENCES

[1] Semiconductor Industry Association, International Technology Roadmap for Semiconductors: 2004 edition (`www.itrs.net/Common/2004Update`) Austin, TX, International SEMATECH, 2004.
[2] Foad M. A. and Jennings D., *Solid State Technol.*, **41** (1998) 43.
[3] Claverie A., Giles L. F., Omri M., de Manduit B., Ben Assayag G. and Mathiot D., *Nucl. Instrum. Methods Phys. B*, **147** (1999) 1.
[4] Wood R. F., Kirkpatrick J. R. and Giles G. E., *Phys. Rev. B*, **23** (1981) 5555.
[5] Narayan J., Holland O. W., Christie W. H. and Wortman J. J., *J. Appl. Phys.*, **57** (1985) 2709.
[6] Tsukamoto H., Yamamoto H., Noguchi T., Masuya H. and Suzuki T., *Jpn. J. Appl. Phys.*, **35** (1996) 3810.
[7] Chong Y. F., Pey K. L., Wee A. T., See A., Chan L., Lu Y. F., Song W. D. and Chua L. H., *Appl. Phys. Lett.*, **76** (2000) 3197.
[8] Whelan S., Privitera V., Italia M., Mannino G., Bongiorno C., Spinella C., Fortunato G., Mariucci L., Stanizzi M. and Mittiga A., *J. Vac. Sci. Technol. B*, **20** (2002) 644.
[9] Whelan S., La Magna A., Privitera V., Mannino G., Italia M., Bongiorno C., Fortunato G. and Mariucci L., *Phys. Rev. B*, **67** (2003) 075201.
[10] Cahn J. W., Coriell S. R. and Boettinger W. J., *Laser and Electron Beam Processing of Materials*, edited by White C. W. and Peercy P. S. (Academic Press, NY) 1980, p. 89.
[11] `http://www.imm.cnr.it/imm/progetti/projects/flash/FLASH_home.html`
[12] La Magna A., Alippi P., Privitera V., Fortunato G., Camalleri M. and Svensson B. G., *J. Appl. Phys.*, **95** (2004) 4806.
[13] La Magna A., Alippi P., Privitera V., Scalese S., Pannitteri S., Fortunato G., Mariucci L. and Camalleri M., *Appl. Phys. Lett.*, **84** (2004) 4738.
[14] La Magna A., Alippi P., Privitera V. and Fortunato G., *Appl. Phys. Lett.*, **86** (2005) 161905.