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A monolithic pixel detector for future HEP experiments

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Summary. — A new idea of a monolithic pixel detector design in a very deep-submicron commercial standard CMOS technology (90 nm) will be presented. The design is based on a lightly doped substrate to obtain a sufficiently thick depletion layer for the detecting element. In particular, the new detecting element is implemented on the same substrate of the innovative analog front-end electronics and the digital architecture to extract and manage the hit information from the pixel cells. The work described in this contribution is the result of a collaboration between INFN, CERN, IN2P3—Strasbourg and C4iMIND (Conseil General de la Haute Savoie).

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1. – Introduction

Pixel detectors for precise particle tracking in high-energy physics have been developed to a high level of maturity during the past decade. We can divide the development of pixel detectors for charged particle detection into two categories: a) hybrid pixel detectors, in which the particle sensitive volume, the sensor, and the readout IC are separate units, and b) monolithic detectors in which the sensor and the readout IC are integrated into one monolithic block. Both types are schematically illustrated in fig. 1.

The large four LHC experiments ALICE [1], ATLAS [2], CMS [3] and LHCb (for the RICH system) [4] use vertex detectors close to the interaction point based on the hybrid pixel technology. The main challenging requirements are: spatial resolution, timing precision and radiation hardness, which is very important for the long-term performance under particle fluencies as high as 10^{15} neq/cm^2. At present, these demands are only met by hybrid pixel detectors which can be considered the "state of the art" in this field of instrumentation.

The monolithic option is very attractive because it can allow a dramatic reduction material budget which is topically in the range 1–3% X_0 for the pixel detectors in use in the LHC experiments. The development described in the following is largely driven by the requirements for the detector upgrades in view of SuperLHC (sLHC) and other

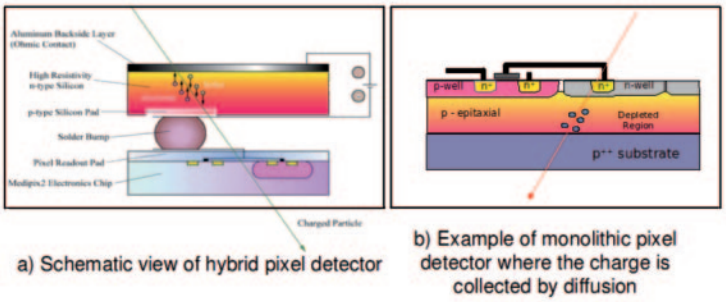

Fig. 1. – Hybrid and monolithic pixel detector architectures.

collider experiments. The monolithic solution to build large surface detectors offers some additional substantial advantages with respect to the hybrid approach, such as: low power consuption, mass production at low cost, reliable production yield.

The actual monolithic pixel detector can be divided in two classes depending on the substrate resistivity: high resistivity, like for instance DEPFET [5] and SOI (Silicon On Insulator) [6]; low resistivity, like for instance the CMOS active pixels (MAPS) [7]. The first type needs non-standard and expensive technological processes which make the volume production difficult. The second type is based on charge collection by diffusion mechanism and uses sequential readout schemes which make it not compatible with sLHC requirements in terms of readout speed. The new monolithic approach presented in this paper merges the main advantages of the actual monolithic pixels with the high performance of hybrid pixel detector. In the following the basic concepts of the integration of the sensor diode with the analog front-end electronics and the chip architecture on a single substrate are described.

2. – Sensor diode

Recently, a commercial foundry has claimed that it can implement a very deep submicron CMOS technology on a moderately doped p-type substrate, which allows an adequate thickness of the depletion layer. An external reverse bias apply to a sensor diode allows to collect the charge by drift and not by diffusion (as in the MAPS). In this way it is possible to reach a depletion region thickness of several tens of micrometers allowing a reasonable signal-to-noise ratio (S/N). Moreover, the high electrical field allows to increase the collection efficiency and to decrease drastically the collection time with consequently reducing charge trapping effects that depend strongly on the radiation levels. On the basis of the above considerations a sensor element with performance comparable with a hybrid detector can be developed and designed. Figure 2(a) shows the basic concept of such a detector.

The integration of the sensor element and the standard CMOS circuit presents many challenges: the signal charge generated by particle must be fully collected in the electrode and not lost elsewhere in the circuit (*e.g.*, on the source or the drain of a transistor); the signal charge should not be dependent on the impact point of the ionizing particle within the pixel cell; the depletion layer should be uniform across the matrix; the reverse bias of the substrate for the sensor diode requires a proper shielding of the circuitry located at the periphery of the matrix. Preliminary 2D device simulations have been performed and the results show that the use of a standard layout approach, like guard

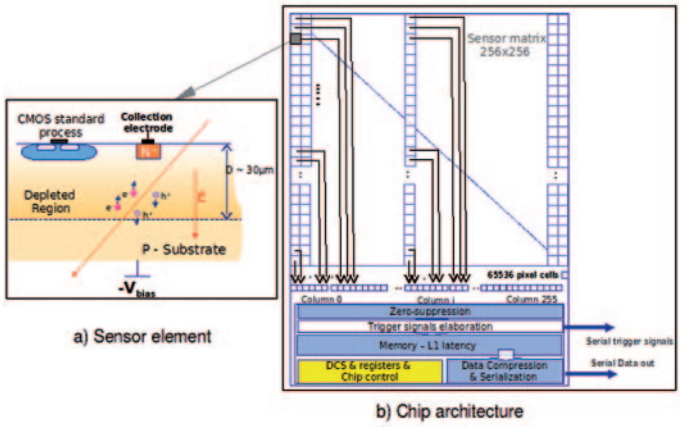

Fig. 2. – Sensor element in CMOS wafer and new chip architecture.

rings, spacing between implants and use of the triple well structures, are sufficient to assure an almost perfectly uniform 30 μm vertical depletion layer. Moreover a good insulation between high voltage and the rest of CMOS circuitry is also feasible. Further studies will be based on 3D simulations for more reliable results. In conclusion, there is a clear indication that the proposed solution is doable and no additional technological steps to the standard CMOS process are required.

3. – Chip architecture

A new readout architecture scheme can be developed on the basis of the progress of the very deep submicron CMOS technologies. In fact, the high metal density in 90 nm CMOS allows to connect every pixel in the matrix to the periphery by means of an individual metal line. This solution allows to make the information of the fired pixels prompt available at the periphery as shown in fig. 2(b).

In the pixel cell only the input transistor is housed while the rest of the analog and digital electronics is located at the chip periphery, thus avoiding the clock distribution through the sensitive matrix because there are no digital blocks located in the pixel cell. The input transistor is directly connected to the sensor diode. The proposed solution has considerable advantages with respect to the currently used designs and technologies, in which signal detection and processing electronics is integrated in the individual pixel cell. The S/N and the power consumption for clock distribution profit of the absence of digital signals distributed over the matrix. Moreover the single transistor in the pixel-cell minimized the number of potential parasitic collection electrodes. A challenge is to keep the area of the readout to a small fraction of the total surface of the chip.

3˙1. *Analog front-end electronics*. – As mentioned previously, the basic pixel cell is made of a collection electrode (n-diffusion diode) connected to the gate of the first p-type transistor device. CAD simulations have shown that the parasitics effects associated to the metal line which connects the analog circuitry to the input transistor can be exploited to shape the signal. Nevertheless these parasitics need to be minimized and the low-k intermetal dielectrics offered in 90 nm CMOS process offer a very significant improvement.

In this proposed solution the S/N depends basically on three parameters: the signal input charge; the input capacitance of collecting electrode and the current drained by the the transistor device, see the following equation:

$$S/N \approx \frac{Q}{C_D} I^m \qquad \text{with} \qquad 1/2 \leq m \leq 1/4,$$

where the exponent m depends on the working region of the transistor, weak, moderate or strong inversion. As a direct consequence of the previous equation, if we divide by n the pixel size, the pixel capacitance is accordingly reduced([1]), by about the same factor n, and correspondingly the S/N will increase. From the previous equation assuming that the $S/N = k$ is constant, the current into the input transistor is given by the following equation and therefore it decreases with the pixel segmentation:

$$I_{\text{TOT}} \approx n \left(k \frac{C_D}{nQ} \right)^{1/m} = \frac{1}{n^{1-3}} \left(k \frac{C_D}{Q} \right)^{2-4}.$$

This opens the possibility for a novel pixel concept with high segmentation and very low power consumption. Preliminary simulations have shown that a good S/N can be achieved with pixel cells dimensions of $100\,\mu\text{m} \times 100\,\mu\text{m}$ (active area) and a power budget limited to about $1\,\mu$W/pixel to be compared with the power consumption of current pixel detectors which is topically one order of magnitude larger. This allows to keep the material budget needed for all services, like cables and cooling, within acceptable limits.

Considering a depletion layer of $10\,\mu$m and a collection electrode capacitance of about 30 fF with $1\,\mu$W, the S/N is about 25. As mentioned earlier we expect to reach larger depletion layer thicknesses, and we believe that the capacitance can be reduced below this value, giving some margin that could be used to save power.

3˙2. *Readout electronics.* – A novel readout architecture is made possible by having the fired pixel information available in the chip periphery at the bunch crossing frequency (*i.e.* 40 MHz for LHC/sLHC). This concept is completely different from the typical current pixel detectors where the information is temporarily stored in the pixel cells until it is transferred at the end of a column of the column-wise organized R/O-chip. The system architecture includes the following subsystems: extraction and zero-suppression data, trigger generation based on specific algorithms, data memory storage, data compression and transmission to the data acquisition. Moreover, a control system is included together with several registers used for threshold, bias, trigger latency, etc. There are also ideas to integrate in the chip several probes to monitor the power consumption, temperature, magnetic field, etc. A possible architecture overview is shown in fig. 2(b). Due to the low occupancy expected in the pixel detectors, in each event a large fraction of cells will be empty. A zero-suppression logic to compress the data volume before the transfer to the back-end electronics, can be developed. The zero-suppression allows to reduce the transmission bandwidth and the power consumption. The overall power budget estimated is around $10\,\text{mW/cm}^2$. The readout architecture of the future pixel detectors will face several challenges, like: a trigger capability based on the tracking information.

([1]) An accurate analysis must include also the parasitic capacitance that cannot be negligible, which limits the segmentation.

4. – Conclusion

The first demonstrator of the proposed devices will be submitted to the foundry before the end of year 2009. This demonstrator will include the sensor diode, the input transistor and some blocks of the analog and digital front-end circuitry. The goal of the first phase is to demonstrate the feasibility of integrating the sensor diode in a matrix on the CMOS wafer with an elementary readout and to demonstrate the efficiency of the sensor element. In addition we are preparing standard test structures to evaluate the radiation tolerance of the transistors in the 90 nm CMOS technology.

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