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Setting-up and calibration of the ALICE Silicon Pixel Detector

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Summary. — The Silicon Pixel Detector (SPD) forms the two innermost layers of the Inner Tracking System (ITS) of the ALICE experiment at LHC. The SPD is the closest detector to the interaction point and therefore it is one of the key detectors for tracking and vertexing capabilities. The SPD is based on hybrid silicon pixel detectors. The detector element, called ladder, consists of a two-dimensional sensor matrix of 256×160 pixel cells bump bonded to 5 ALICE1LHCb front-end chips. The SPD contains 240 ladders and 1200 front-end chips for a total of about $9.8 \cdot 10^6$ channels. The detector response can be optimized by tuning the configuration of several 8-bit DACs embedded in the front-end chip. In this contribution the detector setup and calibration procedures aiming to optimize the detector performance are presented together with the results based on the use of the on-chip programmable amplitude pulser.

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1. – The ALICE Silicon Pixel Detector

1·1. *Introduction.* – ALICE (A Large Ion Collider Experiment) is the LHC experiment devoted to the study of the hadronic matter in extremely high-energy density conditions produced in the ultra-relativistic heavy-ion collisions at LHC (Pb-Pb at $2.75 + 2.75$ TeV per nucleon) [1].

The Inner Tracking System (ITS) consists of six layers of silicon detectors and makes use of three different technologies. The two innermost layers, the closest to the beam pipe, are constituted of hybrid Silicon Pixel Detector (SPD).

The SPD consist of 120 half staves which are made up of two ladders and a Multi Chip Module (MCM) wire bonded to a multilayer bus. The ladder is the active detector element and consists of a bidimensional matrix of reverse biased diodes bump-bonded to five front-end CMOS chips (Alice1LHCb). The front-end chips are divided into 8192 pixel cells having a size of $50\,\mu\text{m}(r\varphi) \times 425\,\mu\text{m}(z)$ [2].

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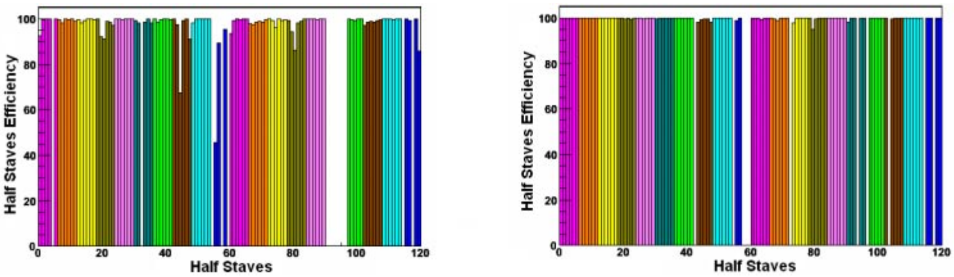

Fig. 1. – Detector efficiency: the two graphs represent the situation of the detector before (left) and after (right) the tuning of the DACs configuration. For each half stave included in the data taking (x-axis), the efficiency in percentage (y-axis) is shown.

1˙2. *Calibrations*. – The commissioning of the SPD started at the end of 2007 and lasted until 2009. A crucial step during the commissioning phase of the detector was the calibration. The working conditions of the pixel chips are optimized by configuring several 8-bits Digital-to-Analog Converters (DAC) embedded in the front-end chips. The purpose of the optimization of these DACs is to achieve the best compromise between performance and power consumption of the detector.

In this phase the attention was focused on the uniformity matrix response of the detector, defined as the pixel matrix efficiency response to the injection of a default charge through the internal pulser. Moreover, during this procedure, noisy and dead pixels are identified and mapped.

A fine tuning of the detector configuration has been done in order to improve this uniformity response. The result of the tuning is shown in fig. 1: the pixel matrix efficiency per half stave is shown before (left panel) and after (right panel) the optimization of the DACs configuration. A partial increase of the efficiency is observed.

2. – Conclusions

The SPD is a key detector for the ALICE data taking. It was installed in June 2007 and since then the commissioning has started. Calibration runs were performed to tune the SPD configuration and to reduce the power consumption without loss in performance. A general increase of the detector efficiency is observed.

Since November 2009 the SPD has actively been taking part in the ALICE data taking with LHC beams, also providing the experiment with a prompt L0 trigger signal.

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