IL NUOVO CIMENTO Vol. 34 C, N. 3 Maggio-Giugno 2011
DOI 10.1393/ncc/i2011-10872-3

Colloquia: Scineghe2010

Cosmic Ray Cherenkov and Fluorescence Imaging: Photosensors and data acquisition systems for a new generation of focal planes

P. Assis([1]), P. Brogueira([1])([2]), O. Catalano([3]), M. Ferreira([1]), L. Mendes([1]), M. Pimenta([1])([2]), P. Rodrigues([1])(*), T. Schweizer([4])(**) and A. Trindade([1])

([1]) *LIP-Lisboa - Avenida Elias Garcia 14-1, 1000-149 Lisboa, Portugal*
([2]) *IST - Avenida Rovisco Pais, 1, 1049-001 Lisboa, Portugal*
([3]) *IASF-Palermo - Via Ugo La Malfa 153, 90146 Palermo, Italy*
([4]) *MPI, Max-Planck-Institute for Physics - D-80805 München, Germany*

(ricevuto il 25 Febbraio 2011; pubblicato online il 12 Maggio 2011)

Summary. — In this paper the design of a new generation of focal planes for Imaging Atmospheric Cherenkov and Fluorescence Telescopes is discussed, based on a Digital Photon Counting architecture instrumented with (SiPM) Silicon Photomultipliers. $3 \times 3\,\mathrm{mm}^2$ SiPMs were chosen to minimize the photoelectron pile-up within intervals shorter than the clock sampling time. The large number of channels requires a compact, modular design with minimal cabling and distance between the photosensors and the frontend electronics. Other design requirements are a high reliability, easy field maintenance and minimization of the total power budget. Data acquisition electronics are partitioned in on-board frontend and off-detector high-level trigger electronics. Extensive use of mixed-signal ASICs and low-power FPGAs for early data reduction were adopted. Temperature is controlled by a liquid cooling sub-system. An asynchronous data readout and filtering, where each of the trigger levels works at its own clock frequency is adopted. The off-detector data acquisition and trigger architecture is based on an asynchronous multi-gigabit switching approach implemented over standard MicroTCA boards, equipped with optical interfaces and high-capability FPGAs. The boards are connected by multi-Gbps optical links to the frontend electronics. Trigger primitives are sent asynchronously to the MicroTCA trigger boards via data links running at their own clocks, for maximum bandwidth. Data and slow-control data streams are sent over the same data lines, reducing in this way the number of cables required. Each crate can process up to 4×10^4 channels and the modularity offered allows further expansion by inter-connecting additional crates with optical fiber links.

PACS 96.50.S- – Cosmic rays.
PACS 29.40.Ka – Cherenkov detectors.
PACS 07.05.Hd – Data acquisition: hardware and software.

(*) E-mail: psilva@lip.pt
(**) Currently at LIP-Lisboa on sabbatical leave.

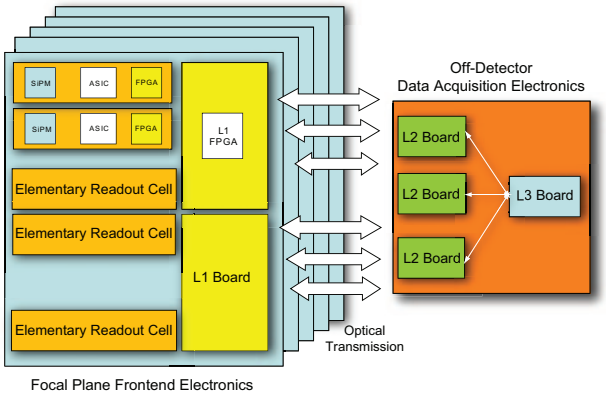


Fig. 1. – Top level SiPM focal plane data acquisition and trigger architecture.

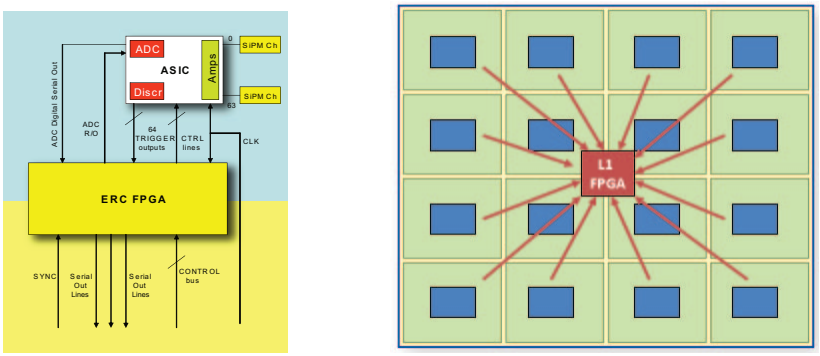
1. – Introduction

The development of a new generation of focal planes is highly desirable in order to improve the overall light detection efficiency, spatial and angular resolution of Cosmic Ray Air Cherenkov and Fluorescence Imaging Telescopes. Due to the potential interest in the application of a new generation of focal planes in experiments such as the Pierre Auger-North [1], the Cherenkov Telescope Array (CTA) [2] or in upgrades to the installed facilities at the Pierre Auger South [3, 4], all of which span vast geographical regions, architectures that include in their design, principles such as high reliability, easy field maintenance with the lowest down-time achievable, and minimization of the total power budget are considered to be highly desirable.

2. – Focal surface design and trigger architecture

The baseline focal plane surface assumes the use of either Silicon Photomultipliers (SiPM) [5, 6] arrays or Multi-Anode Photomultipliers (MA-PMT) [7] with an enhanced single photon sensitivity in the 300–600 nm band, a fast temporal response and a spatial resolution of a few square millimeters. The mechanical and electronics interconnects should follow a modular approach, allowing to build smaller or even combine larger focal planes, while keeping the same frontend and data acquisition electronics. The increase on the number of photosensors due to the reduction of the single pixel area, leads necessary to a larger number of active channels ($4–5 \times 10^4$) requiring a more compact and modular design with a minimal cabling and distance between the photosensors and the frontend electronics. A total power consumption of 1 kW per focal plane is also highly desirable in face of the restricted electrical budget available at most of these experimental sites. In this design, photosensors will operate in Digital Photon Counting [8] in alternative to charge integration approaches. In such working mode, the effects of electronics noise are kept negligible and thus achieving a very high signal-to-noise ratio lowering the trigger threshold [8].

The initial design calls for the focal surface detector to be instrumented with $3 \times 3\,\mathrm{mm}^2$ SiPM pixels organized in 8×8 pixel arrays—fig. 1. The $3 \times 3\,\mathrm{mm}^2$ pixel size is a compromise between minimization of photoelectron pile-up within intervals shorter than the clock sampling time, SiPM pixel production capabilities and the total number of



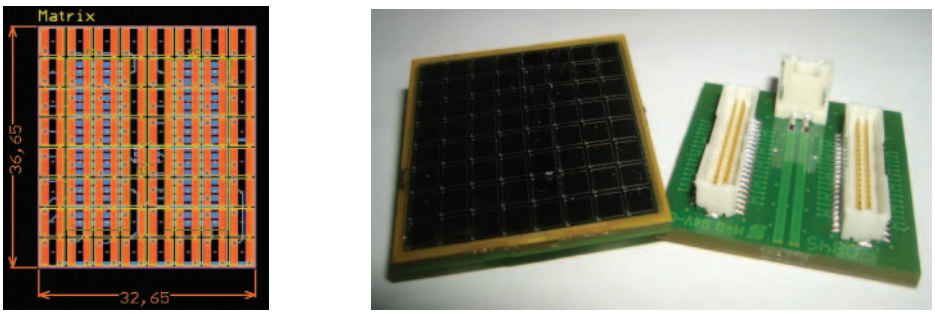
(a) (b)

Fig. 2. – (a) Elementary Readout Cell (ERC) architecture. (b) Physical arrangement of 16 ERC boards into one L1 Sector.

electronic channels. The SiPM readout will be implemented with a 64 input channel mixed-signal ASIC having 64 discriminators for digital photon counting (both single and multiple photon counting are foreseen). A low-power L0 FPGA dedicated to early data reduction will perform zero suppression and implement a local threshold on the number of coincident photoelectron counts in each clock cycle. Both the ASIC and the L0 FPGA will be placed in an Elementary Readout Cell (ERC) board—fig. 2(a). Each ERC will readout one 8×8 SiPM array. At each clock cycle and if above the threshold, a binary image of the position of the active SiPM pixels is transmitted in serial links to the L1 and Data Concentrator board, placed in the focal plane backplane.

2˙1. *L1 Trigger and data concentration.* – The focal plane will be partitioned into multiple independent sectors. Each sector corresponds to a total of 16 ERCs, forming a 32×32 pixel region and is readout by the L1 and Data Concentrator board. Serialized data transmitted from the ERC FPGA is recovered by the L1 Trigger FPGA and the trigger selection applied—fig. 2(b). In each time slot and if the number of active pixels is found to be above the threshold, the L1 Trigger Primitives (timetag and the number of pixels active) are sent to the next level trigger (L2) housed in the off-detector electronics crate. If a trigger accept is issued by the corresponding L2 board the full data payload, consisting of the timetag and the binary image with the location of each active pixel is transmitted to the L2 board for further processing. Both the trigger primitives and the accepted data are moved to the off-detector electronics by means of multi-Gbps optical link—fig. 1.

2˙2. *L2 and L3 Trigger boards.* – Due to a paradigm shift in the data acquisition systems in which traditional parallel bus backplane architectures have been progressively replaced by the emergence of asynchronous multi-gigabit switching approaches, a novel DAQ solution was selected for the readout of these highly pixelated focal planes. The large acceptance by the Telecom Industry of some of the new standards, namely the Advanced Mezzanine Cards [9] for ATCA and MicroTCA [10] data acquisition systems allows to explore commercial off-the-shelf boards, avoiding the design of custom digital boards and concentrating the efforts on the development of data processing and trigger firmware. One of the candidate AMC modules to implement the L2 and L3 trigger



(a) (b)

Fig. 3. – (a) Internal routing of the developed 64 pixel Hamamatsu MPPC carrier board. (b) 64 pixel MAPD3N Zecotek array developed by Zecotek Photonics, Inc.

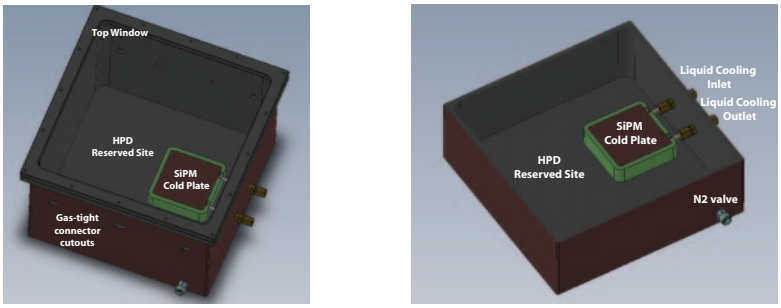
firmware is the BittWare SP/S4-AMC [11]. This AMC is equipped with an Altera Stratix IV GX FPGA with 16 full-duplex, 6.25 GHz SerDes transceivers capable of running 4 optical links up to 3.125 Gbps (SFP) or 6.25 Gbps (SFP+). The several AMCs required to implement the trigger system will be housed on a MicroTCA crate, in which backplane provides rear electrical interconnection between the different L2 and L3 trigger level AMCs. Inter-crate communication is made either by PCI Express 2.0 or Serial RapidIO 2.0. In a standard MicroTCA crate with 10 slots, 9 slots will be equipped with SP/S4-AMCs running the L2 trigger. Each AMC receives data from 4 focal plane sectors, defining a window of 64×64 pixels. On the remaining slot, a 10^{th} SP/S4 AMC, programed with the L3 firmware, receives via the backplane information regarding the L2 Trigger Primitives. In total, up to 36 864 channels from a focal plane with 24×24 SiPM 64 pixel arrays can be processed, corresponding to a total surface area of about $1\,\text{m}^2$.

If in a pre-defined time frame, the number of pixels is above a user-programmable threshold, the L2 AMC sends to the L3 AMC information about the timetag and the number of active pixels. The L3 AMC then combines the information of the number of active pixels and its coarse location (defined by the L2 AMC board index). If a successful candidate passes the final L3 criteria, the relevant information (timetag and individual active pixel locations) held by the L2 boards is sent to the L3 for data concentration and transmission to a computer via one of the front panel optical links.

3. – Feasibility study

3˙1. *SiPM carrier board*. – A SiPM carrier board, with $33 \times 37\,\text{mm}^2$, was designed to house up to 64 Hamamatsu $3 \times 3\,\text{mm}^2$ MPPC pixels (models S10931-100P and S10931-050P [12]) in an 8×8 configuration—fig. 3(a). Individual pixels are organized in a common bias configuration. On the back side of the carrier board, two 40-pin connectors are placed together with an on-board temperature sensor, providing thermal measurements to the slow-control sub-system of the focal plane. In alternative to this carrier board, a 64 pixel MAPD3N array developed by Zecotek Photonics, Inc. and kindly provided to us will also be used in this exploratory phase—fig. 3(b).

3˙2. *SiPM focal plane demonstrator*. – A focal plane technical demonstrator setup was designed in order to test the feasibility of the digital photon counting technique with SiPMs. The gas-tight demonstrator unit can be flushed with N_2 gas, allowing it to be



(a) (b)

Fig. 4. – (a) External view and (b) cut side view of the focal plane demonstrator.

cooled down to $-30\,^{\circ}$C without the risk of water condensation—fig. 4(a). The SiPM carrier board will be placed in thermal contact with a copper plate cooled down by a liquid running fluid—fig. 4(b). On the top side, the unit is closed by a high-transmittance optical entrance window. Provision was also made to install near the 8×8 SiPM array a calibrated HPD Hamamatsu R9792U-40 with a photocathode quantum efficiency of 32–34% at 360 nm [12, 13]. Since SiPMs exhibit a strong variation of the gain and the PDE as a function of the temperature and the bias voltage a two-step online calibration method has been proposed. In the first part a feedback-loop to control the bias voltage of the individual SiPM is implemented by measuring the single photoelectron gain for the dark counts or the night sky background. After the calibrated set of SiPM bias voltages are identified, a 360 nm LED is turned on and the single photoelectron rate from the SiPM pixels compared to the calibrated HPD photoelectron rate in order to estimate the PDE of each SiPM pixel.

3˙3. *Prototype ERC board.* – A prototype ERC board to demonstrate the SiPM single photon counting detection of fluorescence and Cherenkov light, computation of first level trigger primitives, optical transmission, slow-control and environmental monitoring was developed. The SiPM array is readout by a 64 channel MAROC3 ASIC, working at a maximum clock frequency of 80 MHz [14]. Each channel has a variable gain setting and the pulse amplitude is compared against a discriminator, with a minimum threshold of 10 fC at 100% trigger efficiency. The 64 discriminator logic outputs as well as the serial datastream from the MAROC3 ADC are readout by an Altera Cyclone III FPGA. The FPGA performs zero suppression and if in a given clock cycle the number of active pixels (proportional to the number of detected photoelectrons in single photon counting mode) is above an user-defined threshold, data is concentrated and transmitted to SerDes chips capable of data serialization up to 3.125 Gbps and connected to 2 optical fiber SFP transceivers. For debuging and control purposes a RS-232 and a USB2.0 data links were also included. Besides readout and data transmission, the FPGA is also responsible for monitoring the temperature and humidity of the ERC board and of the SiPM carrier board. In addition, two on-board 32-channel 0–5 V DACs are used in order to fine tune the individual SiPM bias voltage.

4. – Outlook

A preliminary concept for a new generation of focal planes was presented. The focal plane will be "photosensor agnostic", instrumented either with the newly developed SiPMs with crosstalk suppression and enhanced PDE as well as with UBA Multi-Anode Photomultiplers. Digital photon counting and highly integrated frontend readout electronics allow to define a $1 \times 1\,\mathrm{m}^2$ lightweight focal plane, with multi-Gbps optical fiber data interconnects and a total power consumption less than 1 kW. A modular DAQ architecture based on Telecom standards was selected to lower the development time and the total cost. Experimental work concerning the characterization of SiPM multi-pixel arrays as well as a prototype frontend and readout board has been initiated. The first experimental tests of the SiPM Focal Plane demonstrator are foreseen for 2011.

* * *

The authors would like to thank colleagues from the Pierre Auger Collaboration for their suggestions and contributions. The authors would also like to acknowledge the assistance of the OMEGA, CNRS-IN2P3 microelectronics design center on the MAROC3 readout ASIC, namely P. Barrillon, S. Bin and C. de La Taille. The authors are grateful to R. Alves and to the LIP-Coimbra Mechanical Workshop for their participation in the design phase of the SiPM Focal Plane demonstrator setup and P. Khaw Kee Keong from Zecotek Photonics, Inc. for providing us with individual MAPD3N and 8×8 arrays test samples. The work of P. Assis, P. Rodrigues and A. Trindade was supported by FCT (Fundação para a Ciência e a Tecnologia) under SFRH/BPD PostDoctoral Fellowships 47707/2008, 37233/2007 and 37226/2007. The work of T. Schweizer was partially supported by a research fellowship from LIP-Lisboa.

REFERENCES

[1] Pierre Auger Observatory, Northern Auger Site, `http://www.augernorth.org/`.
[2] The Cherenkov Telescope Array (CTA) project, `http://www.cta-observatory.org`.
[3] Pierre Auger Observatory, `http://www.auger.org/`.
[4] Abraham J. *et al.*, *Nucl. Instrum. Methods Phys. Res. A*, **620** (2010) 227; doi:10.1016/j.nima.2010.04.023.
[5] Renker D. and Lorenz E., *JINST*, **4** (2009) P04004; doi:10.1088/1748-0221/4/04/P04018.
[6] Anderhub H. *et al.*, to be published in *Nucl. Instrum. Methods Phys. Res.*; doi:10.1016/j.nima.2010.10.081.
[7] Assis P. *et al.*, *Proceedings of the 30th International Cosmic Ray Conference, Mérida, Mexico, 2007*, Vol. **3** (2008), pp. 1519-1522.
[8] Catalano O. *et al.*, *Astropart. Phys.*, **29** (2008) 104; doi:10.1016/j.astropartphys.2007.11.011.
[9] PICMG, PICMG – No. AMC.0 AdvancedMC Mezzanine Module, `http://www.picmg.org/v2internal/resourcepage2.cfm?id=1`.
[10] PICMG, `http://www.picmg.org/pdf/introduction_to_microtca.pdf`.
[11] BittWare Signal Processing Systems, Hills Avenue Concord, NH 03301, USA.
[12] Hamamatsu Photonics K.K., 325-6, Sunayama-cho, Naka-ku, Hamamatsu City, Shizuoka Pref. 430-8587, Japan.
[13] Saito T. Y. *et al.*, *Nucl. Instrum. Methods A*, **610** (2009) 258; doi:10.1016/j.nima.2009.05.075.
[14] Barrillon P. *et al.*, *2007 IEEE NSS MIC Conference Record*, N15-33 (2008).