IL NUOVO CIMENTO Vol. 34 C, N. 6 Novembre-Dicembre 2011
DOI 10.1393/ncc/i2011-11033-6

Colloquia: IFAE 2011

Vertical integration technologies for vertex detectors

L. Ratti

Università degli Studi di Pavia and INFN, Sezione di Pavia - I-27100 Pavia, Italy

(ricevuto il 29 Luglio 2011; pubblicato online il 2 Novembre 2011)

Summary. — This work is focused on the use of vertical integration (3D) technologies in the design of hybrid or monolithic pixel detectors in view of applications to silicon vertex trackers (SVTs) at the future high luminosity colliders. After a short introduction on the specifications of next-generation SVTs, the paper will discuss the general features of 3D microelectronic processes and the benefits they can provide to the design of pixel detectors for high energy physics experiments.

PACS 85.40.-e – Microelectronics: LSI, VLSI, ULSI; integrated circuit fabrication technology.
PACS 29.40.-n – Radiation detectors.

1. – Introduction

Experiments at the future high luminosity colliders (like ILC, SuperB and SLHC) will set severe requirements on each of the parts making up the silicon vertex tracker (SVT), including the detector (*i.e.*, the sensitive silicon volume) and the readout electronics. In order to separate the very dense particle jets emerging from the interaction region, the first detector layer will be placed very close to the pipeline axis and will have to provide remarkably high spatial resolution, with a pitch in the order of 50 μm or smaller. Thin detectors and readout electronic chips, with overall thickness in the order of a few hundred micrometers, will be required for the purpose of minimizing the amount of material in the sensitive region of the tracker, therefore reducing multiple scattering and improving momentum measurement accuracy. These specifications are shown in fig. 1, together with their implications on the design of the readout electronics for pixel detectors and on the technology choice. The use of low mass cooling systems, which is mandatory to comply with the material budget requirements, sets a limit to the maximum acceptable power dissipation in the front-end electronics. A high granularity detector placed at a small distance from the interaction point results in an increased data rate, which may be dealt with by means of sparsified readout architectures, suppressing non-interesting data before they are sent off the chip. Selective data readout requires that some amount of intelligence is included in the front-end electronics and that digital blocks are placed in the

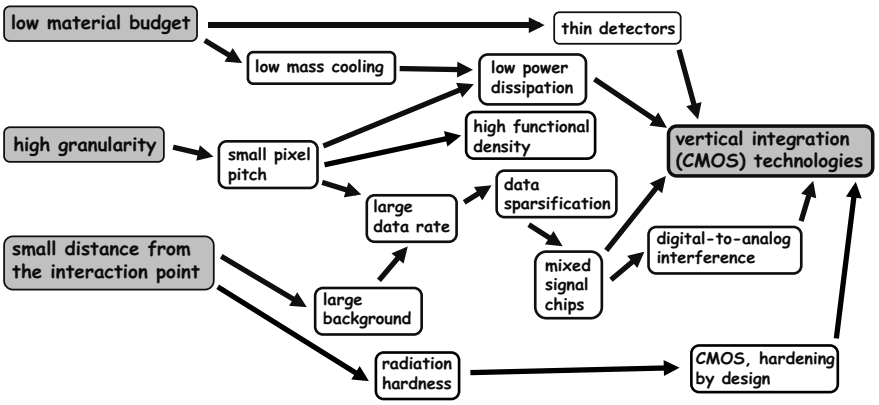

Fig. 1. – Specifications for the SVT at the next-generation colliders and their implications on the design of the detector and the readout electronics and on the technology choice.

elementary cell, together with the analog front-end, and in the chip periphery. In mixed-signal circuits, analog performance may be deteriorated by digital-to-analog interference through the common substrate and/or due to capacitive coupling among signal and power lines. The ionizing radiation levels featured by the detector environment, the harsher the shorter is the distance from the interaction point, set the demand for an accurate radiation-hard design of the readout electronics. Actually, CMOS technologies, together with a well-defined set of design tricks, can provide outstanding performance in terms of tolerance to TID (total ionizing dose) [1]. While not being the only possible solution, vertical integration technologies may satisfy many (if not all) of the above requirements at the cost of some increase in process complexity.

2. – Vertical integration technologies

Vertical, or 3D, integration is an emerging technology that can lead to the fabrication of highly integrated systems by vertically stacking and connecting together various components, in general made of different materials and produced by different processes. There is an intense research activity on the subject in academy and industry throughout the US (MIT Lincoln Labs, IBM, INTEL, SEMATECH, Tezzaron), Europe (CEA-LETI in France, IZM in Germany, IMEC in Belgium) and Japan (T-Micro). Various 3D technologies are currently pursued, but they can be grouped into three main categories [2].

– *Packaging-based 3D integration* is enabled by well-known interconnection methods as wire and bump bonding. It may involve stacking two or more dice one on the other or bonding several dice on a single wafer. As an example, bump bonding technology is typically used in the fabrication of hybrid pixel detectors (which can actually be regarded as 3D devices).

– In *transistor buildup 3D technology*, devices are monolithically integrated on different layers in a single wafer. Depending on the specific process, transistors, besides being integrated in the starting silicon substrate, may be formed a) on a piece of recrystallized silicon film inside the intermetal layers, b) layer by layer on polysilicon films obtained from conversion of amorphous-silicon films or c) layer by layer on single-crystal silicon films.

– *Monolithic, wafer level 3D technology* is enabled by wafer alignment, bonding, thinning and interwafer interconnection, achieved by means of the so-called through silicon vias (TSVs). The various approaches differ as to when the via is formed. In via-first processes, vias are formed before MOS devices, or FEOL (front-end of line); in via-middle processes, vias are formed after FEOL but before completion of wafer fabrication, or BEOL (back-end of line); finally, in via-last processes, vias are formed after BEOL and before or after wafer bonding.

Among the approaches in the list, monolithic 3D technology is the most promising one. With respect to transistor buildup 3D technology, it can take advantage of the features of well-established CMOS processes. Moreover, in the case of heterogeneous integration, separate parts of the design can be fabricated each in the process that best suits its specific needs, then brought together in a vertical stack (for example, one or more CMOS layers for the front-end electronics and a high resistivity substrate for the sensor to obtain a high performance monolithic pixel detector). As compared to packaging-based 3D integration, monolithic 3D technology can benefit from improved mechanical stability, enabling such aggressive post-processing steps as substrate grinding and mechanical polishing (crucial to detector thinning).

3. – Advantages of 3D integration in microelectronic design

Three-dimensional processes are already widely used in the design of high density storage devices and promise to provide a means to overcome the bandwidth bottleneck in modern microprocessors by vertically integrating processor and memory subsystems in a single chip [3, 4]. CMOS imagers in vertical integration technology have also been demonstrated [5]. Three-dimensional integrated circuits (IC), besides obvious size and functional density benefits, can address issues such as signal speed, power dissipation and noise in digital and mixed-signal systems [6]. The speed of the signal in an IC is governed by the transistor gate delay and the RC delay, whose expression, $t_d = 0.35 \cdot rcl^2$, depends on the length l and specific resistance r of the metal wire and on the intermetal specific capacitance c. In deep submicron CMOS technologies, the RC delay has become the predominant contribution to overall signal delay (as interconnect cross section and intermetal layer thickness tend to decrease from generation to generation). As compared to a planar technology, the average wire length in an n-layer 3D IC is theoretically reduced by $\sqrt{n}$, resulting in a propagation delay improvement of a factor of n. In addition, shorter interconnects, with their smaller resistance and capacitance, dissipate less power and require fewer repeater blocks for signal regeneration, which again results in less power consumption. The smaller load capacitance also reduces the noise due to simultaneous switching events and to coupling between signal lines.

4. – Specific potential benefits for pixel detectors

Besides the above-illustrated advantages, which have general relevance for all 3D digital and mixed signal circuits, pixel detectors for vertex tracking applications can benefit from some specific features of vertical integration processes [7].

– Front-end chips for pixel detectors, whether they are monolithic or hybrid sensors, are generally designed in the form of large matrices of individual channels, whose number can range from a few thousand to several tens of thousand. For this reason, readout integrated circuits (also ROIC) in planar technology may suffer

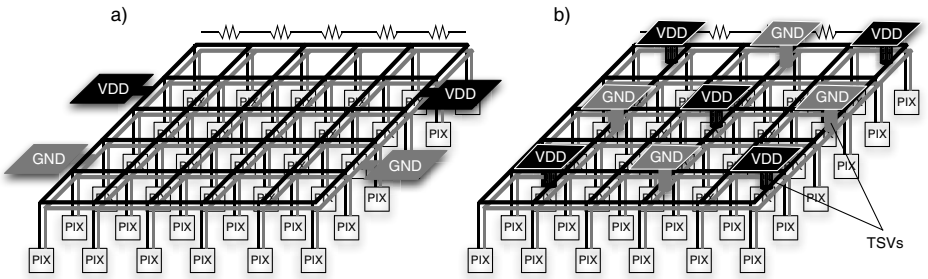

Fig. 2. – Power distribution a) in a 2D front-end circuit and b) as it may be organized in a 3D readout chip (reproduced from [7]).

from voltage drops along metal power lines due to their resistivity, the largest voltage difference being found between the pixels close to the bias pad and those located at the center of the matrix (see fig. 2 a)). As a consequence, readout performance may be found to change from pixel to pixel. In a 3D circuit, power supply pads can be uniformly distributed on the chip back side (opposite to the sensitive side) through suitable metal patterning and connected to the power mesh by means of TSVs (see fig. 2 b)).

– In mixed-signal chips, as is the case for advanced front-end electronics for pixel detectors, one very obvious way to take advantage of 3D integration is by separating the analog from the digital section. As compared to planar microelectronic circuits, where analog stages have to share the same substrate with logic blocks, vertical integration improves the immunity of the analog circuitry to the noise induced by digital activity.

– Three-dimensional structures fabricated through wafer level vertical integration technologies are as stiff as monolithic structures. Therefore, after bonding they can be mechanically processed to reduce the thickness. In the case of a pixel detector, substrate thinning can be exploited to cope with the material budget requirements and improve the momentum resolution of the system. Note, on the other hand, that the classical bump bonding techniques used to fabricate hybrid pixel detectors do not provide sufficient mechanical rigidity for post-processing.

– In a planar readout circuit processing the signals from a matrix of pixel sensors, metal pads are placed along one or more sides of the die to extract data from it and

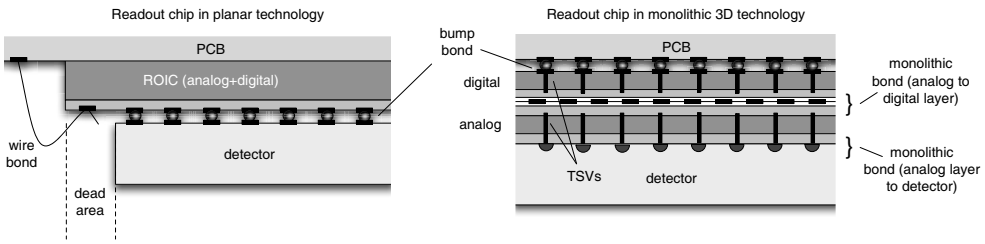

Fig. 3. – Avoiding dead area in the fabrication of pixel detectors by means of vertical integration technologies.

to provide it with programming signals, bias voltages and power supplies. From the standpoint of detection operation, this region of the readout circuit is useless and is generally referred to as the dead area of the chip (see fig. 3). In charged particle tracking applications, and in imaging applications as well, a given surface has to be covered with the minimum amount of insensitive area. This is obtained by suitably overlapping smaller detector units in such a way to cover the dead zone of a unit with the sensitive area of another one. This tiling work, involving precise detector alignment, is some of a laborious process. Vertical integration technologies, on the other hand, make it possible to maximize active detector area by making the readout chip accessible from both faces (see again fig. 3). On the analog side, the ROIC is connected to the detector through monolithic 3D integration techniques while, on the other side, digital readout circuits communicate to the outer world (*e.g.*, a PCB) through bump bonds.

5. – Conclusion and perspectives

Vertical integration technologies may provide several advantages in the development of fast and accurate vertex detectors. The set of processing steps available with 3D monolithic integration (through silicon via formation, adhesive bonding, precise and aggressive thinning, back side metallization and patterning) have the potential for satisfying the severe constraints posed by the experiments at the future high luminosity colliders. Several groups around the world are now working on the first generations of vertically integrated circuits for HEP and scientific imaging applications. Experimental characterization will represent the first testing ground for 3D processes in the field of silicon vertex detectors.

* * *

The author would like to thank all the people in the VIPIX experiment and in the 3DIC Consortium, with whom, for the past few years, he has been collaborating on the development of vertically integrated CMOS circuits for pixel detectors.

REFERENCES

[1] Re V., Gaioni L., Manghisoni M., Ratti L. and Traversi G., *IEEE Trans. Nucl. Sci.*, **57** (2010) 3061.
[2] Lu J.-Q. and Rose K., *Future Fab Int.*, **23** (2007) 25.
[3] Kurita Y., Matsui S., Soejima K., Komuro M., Itou M. and Kawano M., *IEEE Trans. Adv. Packag.*, **32** (2009) 657.
[4] Zia A., Jacob P., Kim J.-W., Chu M., Kraft R. P. and McDonald J. F., *IEEE Trans. VLSI Syst.*, **18** (2010) 967.
[5] Suntharalingam V., Berger R., Clark S., Knecht J., Messier A., Newcomb K., Rathman D., Slattery R., Soares A., Stevenson C., Warner K., Young D., Ang L. P., Mansoorian B. and Shaver D., ISSCC Dig. Tech. Pap. (2010) 38.
[6] Patti R., *Proc. IEEE*, **94** (2006) 1214.
[7] Deptuch G., *Front-end electronics* 4 *3D technologies*, presented at the *Workshop on Vertically Integrated Pixel Sensors, Pavia, Italy, April 22-24 2010*, available at `http://eil.unipv.it/MaKaC/contributionDisplay.py?contribId=27&sessionId=13&confId=0`.