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ATLAS ITk and new pixel sensors technologies

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Summary. — During the 2023–2024 shutdown, the Large Hadron Collider (LHC) will be upgraded to reach an instantaneous luminosity up to $7 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. This upgrade of the accelerator is called High-Luminosity LHC (HL-LHC). The ATLAS detector will be changed to meet the challenges of HL-LHC: an average of 200 pile-up events in every bunch crossing, and an integrated luminosity of $3000\,\mathrm{fb}^{-1}$ over ten years. The HL-LHC luminosity conditions are too extreme for the current silicon (pixel and strip) detectors and straw tube transition radiation tracker (TRT) of the current ATLAS tracking system. Therefore the ATLAS inner tracker is being completely rebuilt for data-taking and the new system is called Inner Tracker (ITk). During this upgrade the TRT will be removed in favor of an all-new all-silicon tracker composed only by strip and pixel detectors. An overview of new layouts in study will be reported and the new pixel sensor technologies in development will be explained.

1. – Introduction

The discovery of the Higgs boson [1, 2] by ATLAS [3] and CMS [3] on July 2012 has been a great triumph for Particle Physics, but many unanswered questions are still open. The LHC should conclude its first life phase (*Phase I*) at the end of 2022 with an integrated luminosity of $\sim 300\,\mathrm{fb}^{-1}$. This will provide answers, but only the High-Luminosity LHC (HL-LHC), with its expected integrated luminosity of $\sim 3000\,\mathrm{fb}^{-1}$ will be able to maximize our understanding. At that time many questions will have to be answered: from the Standard Model completeness to the discovery of new physics that could be around the corner already in LHC Run II that is currently ongoing.

The three major motivators for the LHC Upgrade physics are:

1) Deeper understanding of the Higgs boson (*e.g.* mass, branching ratio, quantum numbers, rare SM decays);

2) Careful measurement of the Standard Model processes to look for hints of New Physics;

3) Explicit searches for New Physics.

2. – Deficiencies of the existing Inner Detector

The ATLAS detector will undergo a significant set of changes during the 2023 upgrade, the plan is set out in the *ATLAS Phase II Letter of Intent* [4].

The current ATLAS Inner Detector (ID) was designed for 10 years of operation, at a peak instantaneous luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, 14 TeV centre-of-mass energy, 25 ns between beam crossings and ~ 23 proton-proton interactions per crossing. The front-end architecture was designed around a single (hardware) Level-1 trigger signal running up to 100 kHz. In HL-LHC will reach 7 times the instantaneous luminosity of LHC Phase I, at this level we will have ~ 200 proton-proton interactions per beam crossing.

Consequently, to sustain the increasing of the trigger rate due to higher luminosity, changes to the trigger architecture are planned. The Level-0 trigger will be moved to 1 MHz with a minimum latency of $6\,\mu$s (designed for at least $10\,\mu$s) and the second hardware trigger (Level-1) at a maximum sustained rate of 400 kHz with minimum latencies of $30\,\mu$s (designed for $60\,\mu$s).

Furthermore in HL-LHC the tracker should operate under high fluences that are related to high radiation damage. The current pixel detector was designed using radiation hard sensors and electronics to withstand the radiation damage that is equivalent to an integrated luminosity of $400\,\mathrm{fb}^{-1}$. Similarly, the Semi-Conductor Tracker (SCT) was designed and constructed to operate up to integrated luminosity of $700\,\mathrm{fb}^{-1}$. This was before the insertion of the Insertable B-Layer.

The Insertable B-Layer (IBL) [5] is a fourth pixel layer, that has been added to the Pixel Detector in 2014 between a new smaller radius beam pipe and the B-layer, at a sensor average radius of 33 mm. The IBL was designed for a fluences equivelent to $850\,\mathrm{fb}^{-1}$. By inserting the IBL, the additional material in the services will increase the fluence in the SCT end-caps by nearly a factor of 2 thus reducing the expected original design lifetime. Therefore, the specifications for radiation tolerance of the detectors in the current ID are significantly below to the $3000\,\mathrm{fb}^{-1}$ that will be collected at the end of the lifetime of the High Luminosity LHC.

Further problems are present in the bandwidth saturation and the occupancy. The front-end electronics of both the pixel and SCT can accommodate events with about 50 proton-proton interactions per crossing and sustained instantaneous luminosity of about $2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, beyond this value limitations in the buffering and the links between the on-module electronics and the read-out driver card (ROD) will lead to inefficiencies [4].

Concerning the occupancy, with the expected pile-up at the HL-LHC the SCT would be unable to resolve close-by particles, and the TRT straws will approach 100% occupancy. Some degradation in the TRT performance has already been observed in the most central heavy-ion collisions.

3. – ITk layout

During Phase II the whole of the inner tracker (TRT and silicon) will be removed, and it will be replaced with an all-silicon tracker which fills the existing tracking volume. The baseline layout for the ITK is presented in fig. 1. An all-silicon-detector tracker is proposed, with pixel sensors at the inner radii surrounded by microstrip sensors. In the central region, sensors are arranged in cylinders, with 4 pixel layers followed by 3 short-strip layers then 2 long-strip layers. The design shown has a $|\eta|$ coverage < 2.7 and guarantees that tracks have at least 11 hits plus an additional redundancy. Many layouts are currently under consideration, with a discussion to extend the tracking coverage to

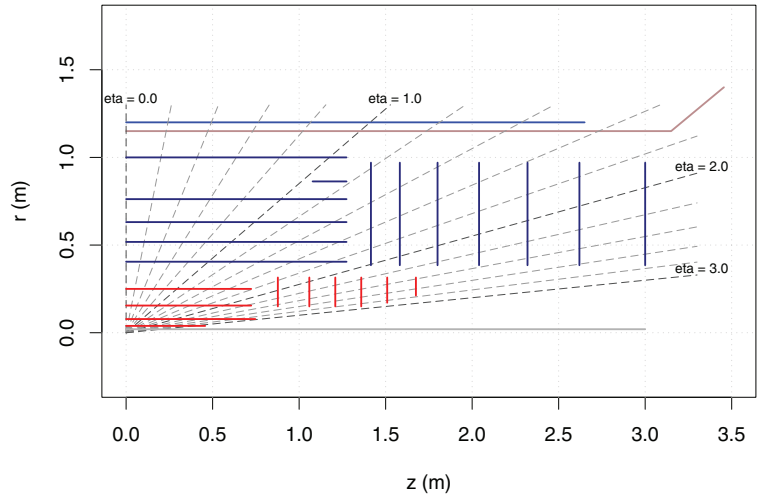

Fig. 1. – The baseline layout of the replacement tracker showing the active areas of silicon detectors arranged on cylinders and disks. Pixels in red and Strips in blue.

$|\eta| < 4$, the final Pixel layout will need to be settled sufficiently in advance of the strip TDR in 2016. The optimal design of the ITk will be a compromise of tracking performance, cost optimisation, ease of construction and installation, as well as the ability to maintain the detector throughout its lifetime.

3˙1. *Expected performances*. – The proposed layout shown in fig. 1 is mainly based on requirements of excellent tracking performance in a high pile-up environment to fully exploit the physics at HL-LHC and in particular to be able to cover 200 proton-proton interactions per beam crossing. As example in table I are reported some characteristics of the performance of the new layout compared with the present inner detector.

4. – Pixel technologies in development

The pixel system technologies currently in consideration for the Phase II upgrade are based on the experience developed and already in use in the ATLAS Pixel Detector [6] and, more recently, in the IBL [5]. New solutions are in study and an intense R&D program is in progress to identify the technological options that could help to improve

TABLE I. – *Performance of the existing ID with IBL, and of the Phase-II tracker for transverse momentum and impact parameter resolution.*

Track parameter $\|\eta\| < 0.5$	Existing ID with IBL no pile-up $\sigma_x(\infty)$	Phase-II tracker 200 events pile-up $\sigma_x(\infty)$
Inverse transverse momentum (q/p_T) [/TeV]	0.3	0.2
Transverse impact parameter (d_0) [μm]	8	8
Longitudinal impact parameter (z_0) [μm]	65	50

the performance or to reduce the overall cost of the tracker. Many aspects have being evaluated and will be resumed in the next subsections.

4˙1. *Sensors*. – In LHC Phase II the sensors will be able to accumulate integrated luminosity until $3000\,\mathrm{fb}^{-1}$ and the inner pixel layers will be exposed to fluence of $1.7 \times 10^{16}\,\mathrm{n}_{eq}\mathrm{cm}^{-2}$ while for outer pixel layers, the expected maximum fluence is $1.4 \times 10^{16}\,\mathrm{n}_{eq}\mathrm{cm}^{-2}$. From the sensor technology at least four possible sensor types are considered for the pixel detector:

1) *Planar sensors* [7, 8] are the oldest technology, but radiation hardness has been proven and mass production capabilities are well established with multiple international vendors. Test-beam results have shown that they can oparate at fluences of more than $10^{16}\,\mathrm{n}_{eq}/\mathrm{cm}^{-2}$. After $2 \times 10^{16}\,\mathrm{n}_{eq}\mathrm{cm}^{-2}$, a bias voltage of 1.5 kV is required for a MIP signal of 6000 electrons. Radiation tolerance sufficient has been also demonstrated for $100\,\mu$m thin n-in-p sensors after a received fluence of $5 \times 10^{15}\,\mathrm{n}_{eq}\mathrm{cm}^{-2}$ at an applied bias voltage of 500 V and for $150\,\mu$m thick sensors after $1 \times 10^{16}\,\mathrm{n}_{eq}\mathrm{cm}^{-2}$ at a bias voltage of 1.2 kV.

2) *3D sensors* [9] require a relatively low depletion voltage even after high irradiation dose, but are currently more expensive due to the more complex technology. In 3D sensors, n- and p-type column-like electrodes penetrate the substrate defining the pixel configuration. The reduced drift path makes 3D devices less susceptible to trapping. During the IBL sensor qualification period, 3D pixel modules irradiated to $5 \times 10^{15}\,\mathrm{n}_{eq}\mathrm{cm}^{-2}$, were operated with excellent hit reconstruction efficiency with a bias voltage voltage of 160 V and moderate cooling requirements. Furthermore, the 3D technology has been proven to be operational at fluences of $10^{16}\,\mathrm{n}_{eq}\mathrm{cm}^{-2}$. Designs with thicknesses of 100 to $200\,\mu$m, with $5\,\mu$m diameter columns are currently being investigated.

3) *Diamond sensors* [10] promise lower capacitance and a high radiation hardness in terms of dark current and so do not require cooling, but are still expensive at the moment and only few vendors are available.

   CMOS Sensors, instead of passive sensors, using a capacitive coupling instead bump-bonding is also in study. ATLAS groups are also involved in the R&D effort on HV/HR-CMOS technology. The deep n-well in a p-substrate is used as the charge-collecting electrode in each pixel cell. It is reversely biased with respect to the substrate. The entire CMOS pixel electronics (amplifier, discriminator, control logic) is placed inside the pixel cell with a reverse bias voltage of 60 V. Signal charge collection occurs mainly by drift and should be radiation hard due to extremely thin sensor depth. After irradiation with low energy protons with a fluence of $10^{15}\,\mathrm{n}_{eq}\mathrm{cm}^{-2}$ and 300 MRad the signal from beta-particles is clearly visible above the noise at moderate temperature. First FE-I4 [11] scale prototypes should be available by the end of 2015.

4˙2. *Front-end electrocnics*. – The ATLAS trigger strategy for HL-LHC proposes two trigger levels of 1000 and 400 kHz and requires a readout of the silicon tracker at 1 MHz. Due the higher requirements on the trigger rate the strategy proposed in the Letter of Intent to use the FE-I4 chip, presently installed in the IBL, for the outermost layers of the ITk Pixel Detector no longer looks reasonable. RD53 collaboration has defined the design goals and new FE chip that will deliver a much better performance. The new pixel

readout chip will go beyond FE-I4 passing through two parallel directions: 3D electronics integration and 65 nm feature size conventional CMOS. A readout cell size of $50 \times 50\,\mu\text{m}^2$ (compatible with $50 \times 50\,\mu\text{m}^2$ or $25 \times 100\,\mu\text{m}^2$ pixels) is being targeted in order to have high resolution on the track impact parameters, avoid cluster merging for better two-track resolution and reduce occupancy for high efficiency and low fake rates. The RD53 chip is now considered the baseline for all the layers of the Pixel Detector. A first prototype is expected in the second part of 2017.

5. – Conclusions

The LHC Run II at 13 TeV centre-of-mass energy is ongoing and we are optimistic that unexpected physics signatures might be found. An overview of the main upgrade of the ATLAS tracking detector has been given, but upgrades will be made in computing, databases, and the front-end electronic systems for most the sub-detectors within ATLAS [4]. The new ATLAS Inner Tracker will be an extraordinary technological effort for R&D laboratories and vendors, but will certainly able to meet the challenges of the HL-LHC.

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