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MAPS application for the ITS upgrade

A. LATTUCA on behalf of the ALICE COLLABORATION
Physics Department, University of Torino and INFN, Sezione di Torino - Torino, Italy

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Summary. — The Monolithic Active Pixel Sensor (MAPS) technology is of central interest for the innermost tracking layers of particle physics experiments since they enhance the detector granularity and thus allow for very high spatial resolution with low material budget. This contribution will focus on the MAPS implementation for the ALICE ITS Upgrade. Within the ongoing R&D program, the ALPIDE chip is under development with a wide pixel matrix consisting of 512 rows and 1024 columns. With this high pixel granularity a fast read out is mandatory. For this purpose a high speed serial link, which works at the targeting speeds of 1.2 Gbps/400 Mbps, is integrated in the chip in order to send out data at the far end of a differential cable. To overcome the physical limitations imposed by the signal lines and properly reconstruct the signal, pre-emphasis technique is mandatory at such long distances. This contribution summarizes the ongoing studies on the data transmission quality and presents the first measurement of the first produced prototype.

1. – ALICE ITS Upgrade - Background and Motivation

ALICE is a general-purpose detector with which the physics of the strong interacting matter and the characterization of the quark-gluon plasma by means of the Pb-Pb and p-p collisions are studied. The ALICE system consist of different kinds of detector technologies. In particular, the nearest detector to the interaction point is the Inner Tracking System (ITS) which is used to localize the primary vertex of interaction, reconstruct the secondary vertex and identify the low-p_T particles which traverse the detector.

The ITS surrounds a 800 μm beryllium beam pipe with 6 cylindrical layers made of different silicon detector technologies, as summerized in table I [1].

Those detectors are radiation hard, in order to deal with the ALICE radiation dose, and provide informations on the x and y coordinates of a particle hit.

In view of the LHC upgrade after the Long Shutdown 2 (LS2), the instantaneous luminosity for the Pb-Pb collisions will increase up to $\mathcal{L} = 6 \times 10^{27}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. For this reason even the ITS will be upgraded to overcome the two major limitations of the current system which concern the read out rate capabilities and the poor impact parameter

TABLE I. – *The Current Inner Tracking System.*

Layer	Type	r (cm)	$\pm z$ (cm)
1	Hybrid Pixel	3.9	14.1
2	Hibryd Pixel	7.6	14.1
3	Drift	15.0	22.2
4	Drift	23.9	29.7
5	Strip	38.0	43.1
6	Strip	43.0	48.9

resolution. Actually, a read out rate capability limited to 1 kHz is not sufficient to deal with a 50 kHz interaction rate foreseen for the LHC upgrade. Furthermore, the high material budget of overall detector does not allow to properly reconstruct the tracks of the short-lived particles.

1˙1. *The upgrade strategy.* – The upgrade strategy is based mainly on the use of Monolithic Active Pixel Sensor that will improve the impact parameter resolution, the tracking efficiency and momentum resolution for low-p_T particles. Furthermore, a new read-out architecture to read out data related to each individual Pb-Pb interactions will be implemented. After the LS2 in 2018, the new ITS will have the characteristics summarized in table II [2].

The working principle of a MAPS is based on the depletion of a p-n junction in a standard CMOS process. The collection diode is a n-well implant on top of a 10–18 μm thick p^+-epitaxial layer which is the sensitive volume. A MIP which traverses the sensor will generate in this small volume about 1600 electrons which will be collected mainly by diffusion. This is the major drawback of a standard MAPS since collection by diffusion is a relatively slow process which degrades the collection efficiency and the radiation hardness of the device. Furthermore, the n-well collection diode prevents the implementation of complex in pixel circuitry. Actually, an additional n-well for the implant of a PMOS will degrade the MAPS charge collection efficiency because it will compete with the sensing diode for the charge collection. However, a MAPS allows to have thinner devices since the sensor and the read-out electronics are built on the same silicon wafer, thus reducing the material budget and therefore it is a suitable option for the ITS upgrade [3]. On fig. 1(a) a standard MAPS is shown.

TABLE II. – *The New Inner Tracking System.*

		Layer	Type	r (cm)	$\pm z$ (cm)
Inner Barrel	Inner Layer	0	MAPS	2.24–2.67	27.1
		1	MAPS	3.01–3.46	27.1
		2	MAPS	3.78–4.21	27.1
Outer Barrel	Middle Layer	3	MAPS	19.44–19.77	84.3
		4	MAPS	24.39–24.70	84.3
	Outer Layer	5	MAPS	34.23–34.54	147.5
		6	MAPS	39.18–39.49	147.5

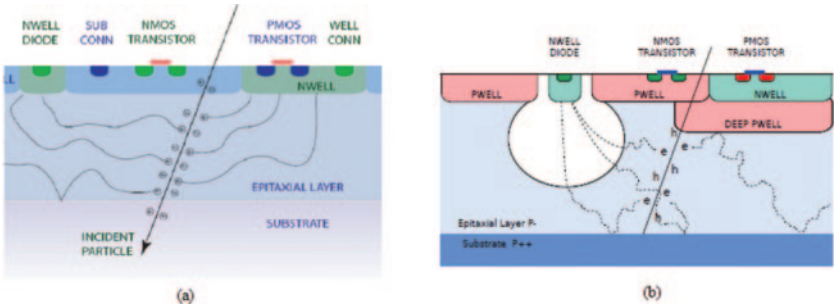


Fig. 1. – (a) Layout of a Standard MAPS [1]. (b) Layout of a MAPS with the quadruple well [5].

1˙2. *A MAPS application for the ITS upgrade.* – The aim of the ITS upgrade is to have a pixel chip which satisfies demanding constraints about the power consumption and the integration time. Actually, a power consumption $< 100\,\mathrm{mW/cm^2}$ and an integration time $< 30\,\mu\mathrm{s}$ are the requirements for the new ITS pixel chip detector [5]. On this basis, the overall ITS R&D program is based on the use of TowerJazz 0.18 μm CMOS technology mainly because MAPS with the Quadruple-well option are produced. As shown in fig. 1(b) with this option a deep p-well is underneath the n-well which hosts the PMOS. In this way inside the sensitive volume an electrical filed is generated which prevents those n-well from collecting charge and, in the meanwhile, it guides the charges toward the sensing diode. Together with this key feature, the TowerJazz 0.18 μm CMOS technology is more robust to the radiation effects, thanks to the transistor feature size and 4 nm gate oxide thickness [4]. Furthermore, a high resistivity epitaxial layer is available, for which the resistivity is ranging between 1 and 6 kΩ·cm, so that a sizable part of the sensor can be depleted. The application of a moderate reverse bias will enhance further the charge collection performance because more charge is collected via the drift mechanism thus reducing the collection time.

2. – The ALPIDE chip

ALPIDE stands for ALICE Pixel Detector and it is the pixel chip developed by the INFN VLSI design team of Torino together with CERN, CCNU and Yonsei as one of the possible design option for the ITS upgrade. Actually, the objectives of the ALPIDE design are a bit more aggressive than the ITS requirements since it will have a power density less than $30\,\mathrm{mW/cm^2}$ and an integration time below $3\,\mu\mathrm{s}$ [5]. ALPIDE consists of a 512×1024 pixel matrix and a pixel chip periphery for a total $3.0 \times 1.5\,\mathrm{cm^2}$. In the present prototype the pixel matrix is divided into four sectors which have different sensor geometries. The hit pixels are red by a data-driven readout architecture with zero-suppression in the matrix. The pixel chip periphery is dedicated to the slow control and clock distribution as well as the high speed data transmission circuitry.

2˙1. *High-Speed Data Transmission.* – The High-Speed Data Transmission Unit (DTU) is made by a ×15 multiplier Phase Locked Loop, a high speed Serializer and a pseudo-LVDS driver. This last component sends the data in a digital form to the patch panel which is located at the far end of a twinax coaxial cable. ALPIDE has an high granularity pixel matrix so it needs a fast read-out in order to deal with a 50 kHz interaction rate foreseen for the LHC upgrade. From the architectural studies, to efficiently read the entire matrix the transmission speeds at which the data have to be sent out of

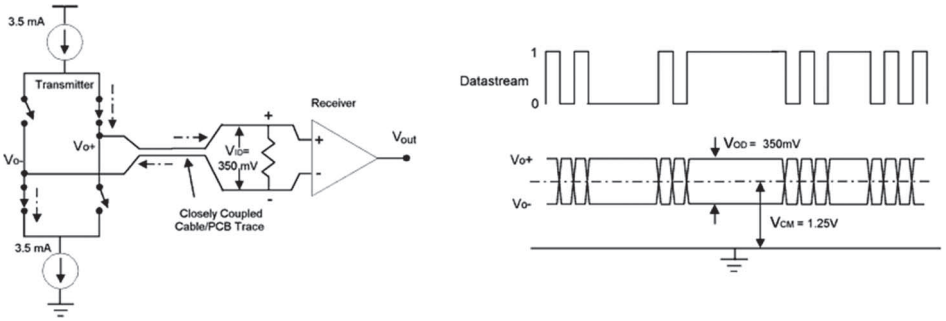


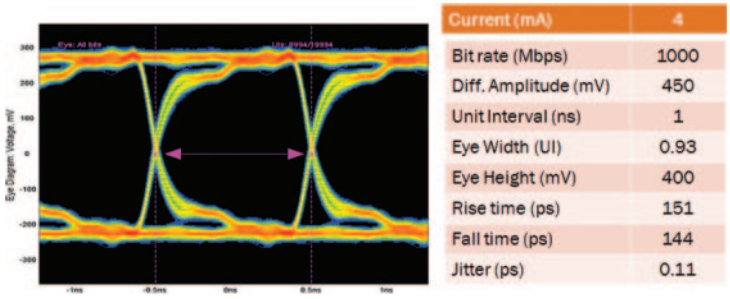
Fig. 2. – Low-Voltage Differential Signaling (LVDS): working principle [6].

the chip are 1.2 Gb/s and 400 Mb/s for the Inner Barrel and Outer Barrel, respectively. Those are the speeds at which the pseudo-LVDS driver has to run, by driving a 5–6.5 m long transmission line. The design challenge here is to overcome the RC limitations imposed by the transmission line in order to have a good transmission quality at the end of the cable.

2˙2. *Low-Voltage Differential Signaling Transmission.* – The Low-Voltage Differential Signaling (LVDS) is the transmission protocol that has been chosen to deal with the high data rate since it allows for very high transmission rate with low power consumption. The standard ANSI/TIA/EIA-644 summarizes the electrical characteristics of this protocol. Essentially, a LVDS system is made by a driver, which drives a differential line, and a receiver, which is sensible to the difference between its inputs. This approach takes the advantage of a differential transmission since it is less sensible to the common mode noise and the electromagnetic interference. The receiver inputs are terminated with a 100 Ω termination resistor in order to avoid signal reflection to the driver outputs. Furthermore, the low voltage swing at the driver output enhance the transmission while saving power [6]. The common way to evaluate the transmission quality is to use the eye diagram, which gives quantitative and qualitative informations about the transmission. This envelop (see fig. 2) is mainly characterized by its horizontal aperture (eye width), vertical aperture (eye height), Unit Interval (UI) and by the jitter amount. Whilst the UI defines one data bit-width, the jitter is defined as "the short term variation of significant instants of a digital signal from their ideal positions in time" [7]. Generally speaking, a transmission quality is acceptable if the total jitter is < 0.3 UI.

3. – Pseudo-LVDS output driver for the ALPIDE chip

The first prototype of pseudo-LVDS driver designed for the ITS is based on the one presented in [8]. It works in current steering mode by driving a DC current which can be set between 2 and 4 mA. In this case the common mode was set to 1.1 V to deal with the 1.8 V power supply. This prototype was produced in a separate test chip and tested in 2013 up to 1 Gb/s. Some measurement results are reported in fig. 3. Even if the test results of the first prototype were promising, the driver circuit has been modified in order to reach the target speed of 1.2 Gb/s over a 5 m long semi-custom transmission line. The transmission with this long cable is the main issue during the driver design since the electromagnetic field, which is propagating there, can be reflected because of the impedance mismatches along the line.



Current (mA)	4
Bit rate (Mbps)	1000
Diff. Amplitude (mV)	450
Unit Interval (ns)	1
Eye Width (UI)	0.93
Eye Height (mV)	400
Rise time (ps)	151
Fall time (ps)	144
Jitter (ps)	0.11

Fig. 3. – Test results at the transmission speed of 1 Gb/s with a 50 cm long differential cable.

3˙1. *Pre-emphasis technique.* – In order to overcome the RC limitations imposed by the long cable and properly reconstruct the signal at the end of it, the driver strength has to be high enough so that the energy loss in the cable can be neglected. For this reason pre-emphasis (PE) technique has been adopted by implementing a PE driver. The PE principle consists of an increase of the signal amplitude for a very short time in correspondence of the signal transition, in order to increase the system bandwidth. It will be activated when, for each logic level transition, two subsequent signals are different. In this case the PE driver drives a extra current on the line. This extra current contribution ranges between 1 and 2.5 mA. The driver with the PE driver have been fully simulated and it is currently under test in a separate test chip from ALPIDE. Recently, the full DTU has been integrated in the last version of the ALPIDE chip and in a separate test chip and the first test results will be executed in September.

4. – Summary

MAPS are a suitable solution for the innermost tracking layers of the ALICE ITS. Actually, they allow for high granularity and low material budget detectors. For the ITS Upgrade the TowerJazz 0.18 μm CMOS imaging sensor process has been chosen since it offers MAPS sensor with the quadruple well option. For that purpose, the ALPIDE chip is under development. This chip has such a high pixel granularity that a fast read-out of the matrix is mandatory and the DTU block has been designed to this function. In particular, the high speed pseudo-LVDS output driver runs at the target speeds of 1.2 Gbps/400 Mbps to send data out of the chip at the far end of a differential cable. To overcome the physical limitations given by the signal lines and properly reconstruct the signal, pre-emphasis technique has been adopted, thus enhancing the transmission quality.

REFERENCES

[1] ALICE Collaboration, *Conceptual Design Report for the Upgrade of ALICE ITS Technical Report* -CERN-LHCC-2012-013,LHCC-P-005 (Aug 2012).
[2] Musa L., *ALICE Inner Tracking System (ITS) Upgrade Overview - 4th ALICE ITS, MFT and O2 Asian workshop* (Pusan, South Korea).
[3] Snoeys W., *Nucl. Instrum. Methods Phys. Res. A*, **731** (2013) 125.

[4] Hillemans H. *et al.*, *Radiation hardness and detector performance of new 180nm CMOS MAPS prototype test structures developed for the upgrade of the ALICE Inner Tracking System*, *Nuclear Science Symposium and Medical Imagin Conference (NSS/MIC)*, (2013) IEEE.
[5] ALICE Collaboration, *Technical Design Report for the Upgrade of the ALICE Inner Tracking System*, Technical Report "CERN-LHCC-2013-024 (Nov, 2013).
[6] Texas Instruments, *LVDS Owner's Manual* `www.ti.com/LVDS` (2008).
[7] Peng Lii Mike, *Jitter, Noise, and Signal Integrity at High-Speed*.
[8] Tajalli A. and Leblebici Y., *IEEE J. Solid-State Circ.*, **44** (2009) 2.