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ATLAS pixel detector: Readout upgrades for Run2 and beyond

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Summary. — For a few years, and in major extent in the upcoming future, a series of upgrades of the Large Hadron Collider at CERN have been pushing to the limit the ability of the present detector hardware to efficiently collect data. It is therefore necessary, for most of the detectors subsystems, to keep pace with this development and to foresee the future challenges of high energy physics. The pixel detector of the ATLAS experiment is not excepted and, together with the implementation of a new detector layer in addition to the existing ones, it is necessary to upgrade the data acquisition system (DAQ) of the detectors used efficiently until now to cope with the increased instantaneous luminosity and to avoid harmful pile-up effects.

1. – Introduction

During the data-taking phase Run1 of LHC (2009–2013), the ATLAS pixel detector proved to be a trustworthy ally on data reconstruction. After a long shutdown of two years, the second phase (Run2) has started with an increase of center-of-mass energy from 8 TeV to 13 TeV (near the design nominal maximum of LHC of 14 TeV), a reduction of the bunch spacing from 50 to 25 ns and with a progressive rise in luminosity from $6 \cdot 10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ to beyond $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. These new conditions require an evolution of the data-taking system of the pixel detector, as well as the detector itself.

The structure of the pixel detector for Run1 was composed of three layers of sensors (B-Layer, Layer 1 and Layer 2, in this order from the beam axis to the outer part of the detector) providing high-resolution tracking information on the passage of charged particles in the region of pseudorapidity $|\eta| \leq 2.5$. During spring 2014 a fourth layer, the Insertable B-Layer (IBL) was added at a distance of 33.4 mm [1] from the beam, providing a higher-resolution information to improve the tracking performance.

IBL is composed of 14 staves, each one equipped with 32 front end readout chips (FE-I4) [2], direct evolution of the previous FE-I3 chip [3]. In order to keep at pace the existing Layer 1 and Layer 2, the technology and the experience developed during Run1 and IBL commissioning are used to update the DAQ System of these parts of the

detector. This upgrade is concluded for Layer 2, using the IBL read-out boards (IBLROD e IBLBOC), as well as custom hardware (Optical Transceiver Plugins) designed for this system. Layer 1 will be upgraded in the same way in the next future, while B-Layer can not be further upgraded as the bandwidth is already at the limit; moreover it is anyhow foreseen to become less efficient due to the heavy radiation damages suffered being close to the beam.

2. – PIXEL/IBL DAQ

2˙1. *Pixel modules*. – IBL and Layer 1/2 use different read-out front-ends for the data collection, namely FE-I4 and FE-I3, respectively. When a charged particle passes through the pixels (18×160 (2880) readout channels per chip in the FE-I3 and 80×336 (26880) in the FE-I4) it creates a ionization signal that is collected by the front-end electronics and converted into an optical signal via an "optoboard".

2˙2. *Electro-optical transceivers*. – The optical signal is acquired by an electro-optical transceiver mounted on a "Back-Of-Crate" (BOC) board. The electro-optical transceiver is a custom solution, SNAP 12 compatible, designed in order to sustain 160 MHz Non-Return to Zero (NRZ) operations, while having the possibility to modify the signal threshold channel by channel.

The working region (signal threshold *vs.* input optical power space) has been tested performing extensive BERTs (Bit Error Rate Test) @ 80 MHz requiring to each point to correctly read back data with 100% integrity for 10^{13} bits. To prove the stability over time, the transceivers have been put in working condition during an ageing test (80 °C e 80% relative humidity), to simulate 10 years of operation at 25 °C and 20% of relative humidity.

2˙3. *IBL Back-Of-Crate/IBL Read-Out Driver boards*. – The two data-taking boards are based on the old Pixel equivalents (PixROD and PixBOC) but with wide improvements, mainly due to the use of the FPGA technology instead of DSP units. The IBL BOC receives the optical data from the pixel modules and, after the opto-electrical conversion, sends it to the ROD board where is formatted. It also provides timing for the ROD/BOC pair. Each BOC converts 32 streams of incoming data, divided internally in two channels each of which is controlled by a Spartan-6LX150T FPGA. The two FPGAs (BMF) are controlled by a central master (BCF) Xilinx Spartan-6LX75T.

The IBL ROD has both control functions, sending configuration, reset and trigger signals to the detector, and data format functions. After receiving data from the BOC, it builds a "fragment" that is sent via the S-Link interface to the analysis and storing system. Like the BOC board, this is performed in parallel on 32 streams divided into two input channels by two Xilinx Spartan 6 LX150-FGG900 slaves, while a Xilinx Virtex 5 FXT70T-FF1136 FPGA works a system master.

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