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Image processing applications: From particle physics to society

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Summary. — We present an embedded system for extremely efficient real-time pattern recognition execution, enabling technological advancements with both scientific and social impact. It is a compact, fast, low consumption processing unit (PU) based on a combination of Field Programmable Gate Arrays (FPGAs) and the full custom associative memory chip. The PU has been developed for real time tracking in particle physics experiments, but delivers flexible features for potential application in a wide range of fields. It has been proposed to be used in accelerated pattern matching execution for Magnetic Resonance Fingerprinting (biomedical applications), in real time detection of space debris trails in astronomical images (space applications) and in brain emulation for image processing (cognitive image processing). We illustrate the potentiality of the PU for the new applications.

1. – Introduction

Pattern recognition problems are very common in data processing and the quality of the results is strongly correlated to the efficiency and power of the used computing devices. Pattern recognition implementations are used as a pre-processing step in various highly demanding computational problems to provide a data reduction process with minimal information loss. These problems call for data processing of huge amounts of data (big data problems) with strict, very demanding and often real-time performance requirements.

In this paper we present an innovative embedded system for real-time pattern recognition. The system is an adapted and "miniaturized" version of a hardware system developed for the field of High Energy Physics and more specifically for the execution of extremely fast pattern matching for tracking of particles produced by proton-proton collisions in hadron collider experiments.

The system works as a contour identifier based on the principles of cognitive image processing [1], which means that the implemented pattern matching algorithm mimics the operation of the human brain. This process can be implemented in 2D and 3D image processing for black and white or grayscale images. The hardware acceleration provided by the proposed system can be especially useful in 3D processing of for biomedical applications such as PET and MRI.

2. – Algorithm and hardware implementation - results

A multilevel model is proposed as appropriate to describe the brain image processing. The human brain, when under stress or in situations of danger, dramatically reduces the input visual information by selecting for higher level processing and long-term storage only data that match a specific set of patterns. They are selected by using the principles of information theory (Boltzman entropy [1]) to choose the patterns that contain the most useful information under the constraints of finite computing power and finite output bandwidth ("relevant patterns"). These constraints are compatible with the constraints used in embedded systems for memory size and data throughput.

To implement this system we use a powerful combination of FPGAs and the full custom associative memory chip (AM) [2]. The AM is a content addressable memory like ASIC that executes pattern matching with maximum performance and utmost gate integration. In the presented system the patterns are 3×3 pixel squares in the 2D case or $3 \times 3 \times 3$ pixel cubes in the 3D case.

The system's implementation is divided into two parts: a) the training phase and b) the real-time pattern recognition phase. In the training phase a suitable sample of images (*e.g.* more than 1000 for the 2D B/W case) needs to be processed to select the "relevant patterns". The entropy of each pattern is calculated and the ones selected are those that correspond to the entropy maximum. The chosen patterns are then loaded in the AM and used as a reference to execute pattern matching. The output of the system is an image with clearly identified contours. Various post processing algorithms can be used (such as pixel clustering) depending on the application.

The training and the post processing functions are executed on the FPGA. We have chosen a Xilinx Kintex Ultrascale XCKU040 of a KCU105 evaluation board, easily connectible to an external PC (or a video camera) and to a set of AM chips. The training phase is implemented and tested for 2D B/W images and the complete training implementation uses less than 2% of the FPGA LUTs and 2.4% of the available BRAMs. Using a 250 MHz clock we process a 512×512 pixel image in less than 2.5 ms, more than 1000 times less time than required by a i5 processor for the same image.

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