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Development of the multicell SDD for Elettra and SESAME XAFS beamlines

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Summary. — We report on the first tests of a new prototype fluorescence detector in development for the XAFS beamlines at Elettra (Trieste, Italy) and SESAME (Amman, Jordan) synchrotrons. The beamlines operate in the energy ranges 2–27 keV and 4–30 keV, respectively. The new detector system is based on Silicon Drift Detector (SDD) and SIRIO ultra-low–noise front-end ASIC. The custom-made detector, front-end and back-end electronics system are designed specifically on the beamlines requirements and developed within the framework of the INFN ReDSoX collaboration. The SDD sensors are produced in collaboration with FBK.

1. – Introduction

The XAFS beamlines at Synchrotrons provide chemical and physical information about the atomic electron structure of materials by combining X-ray absorption spectroscopy (XAS) with X-ray diffraction (XRD). In a typical XAFS beamline radiation is Bragg diffracted on a double-crystal monochromator and irradiates a specimen placed between two ionization chambers that allow the absorption coefficient to be studied near the edges. When a specimen is optically thick to X-rays or if the element of interest is too diluted, then the fluorescence technique is used in place of transmission. In this work we report on the development activity and first tests of the new fluorescence detector prototype that will equip the XAFS beamlines of Elettra (Trieste, Italy) and SESAME (Amman, Jordan) synchrotrons. The beamlines operate in the energy ranges 2–27 keV and 4–30 keV, respectively. Due to the particular conditions of the XAFS fluorescence measurement the beamlines require a custom detector properly designed to reach an adequate energy resolution (150 eV at 6 keV) while providing a low dead time for a high count rate. A typical photon flux of 10^9–10^{12} photons s^{-1} cm^{-2} impinges on the specimen that comprises usually a matrix of different elements in addition to the one of interest. All of them are typically excited and emit fluorescence radiation whose flux depends on the element fluorescence yield (for example for typical elements of interest as sulfur, iron

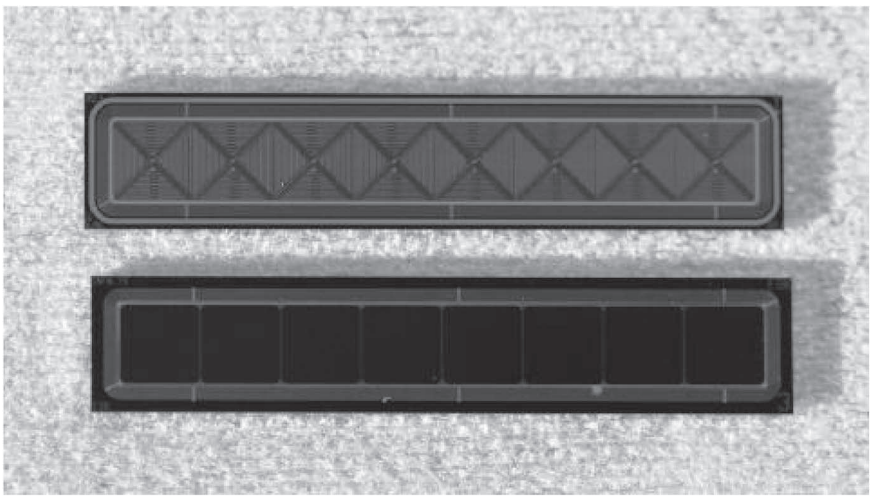

Fig. 1. – The SDD sensor of the detector head comprising 8 cells $3 \times 3\,\mathrm{mm}^2$. On the top the anode side is shown, on the bottom the entrance window.

and copper it is about 10%, 30% and 40%, respectivelly). In addition the scattering of X-rays occurs on the set-up and spreads photon energy across the spectrum. Therefore only a very small fraction of the emitted radiation from the specimen comes from the elements of interest. Currently the fluorescence measurements at Elettra are performed by means of a KETEK GmbH AXAS-M Silicon Drift Detector. It has a single $100\,\mathrm{mm}^2$ SDD cell ($80\,\mathrm{mm}^2$ of effective area with collimation) with an FWHM energy resolution of $\sim 170\,\mathrm{eV}$ for the Mn $K\alpha$ line at $5.89\,\mathrm{keV}$ for a peaking time of $1.32\,\mu\mathrm{s}$ at $-70°$. It reaches up to 50% of dead time with $1.3 \times 10^5\,\mathrm{counts\,s}^{-1}$ of output. Such a set-up is limited at high count rate by dead time due to the monolithic geometry of the Si sensor. A new detector comprising a segmented sensor coupled with a fast electronics allowing $\sim 1\,\mu\mathrm{s}$ shaping time is needed to match the requirements of the measurement technique. Each segment should be a small cell that constitutes also the sensitive element of an independent read-out channel. We developed a simulation software based on the GEANT4 toolkit [1] to optimize the detector design. The simulator reproduces the typical set-up of a XAFS beamline and generate the source energy spectrum, given the ring current properties. From the simulation we estimated that a detector channel with a sensitive element of $9\,\mathrm{mm}^2$ is able to obtain a count rate of $5 \times 10^4\,\mathrm{counts\,s}^{-1}$, compliants with the beamline requirements. Thus, the SDD sensor (see fig. 1) is designed as an array of 8 squared cells $3{\times}3\,\mathrm{mm}^2$ such that an $8{\times}8$ matrix can be built by stacking them along the long side and obtain a total collecting area of about 576 mm^2, seven times larger with respect to the current detector at Elettra. The small area of a single cell allows also to have a low leakage current typically as low as 10 pA that allows to perform measurements with a moderate cooling (at temperature not lower than $-10\,°\mathrm{C}$).

This new detector is based on the state of the art technology both on the sensor and electronics side. The SDD sensors are obtained from high resistivity n-type silicon wafers $450\,\mu\mathrm{m}$ thick. They are designed by INFN-Ts and manufactured by FBK. Each cell collects the ionization charges produced by the photoabsorption by drifting them towards the anode (small n^+ pad) at the centre on the back side. The drift cathodes on the back side are arranged as a decreasingly negative biased p^+ rings. The outermost of

them is kept at the bias voltage and a voltage divider is integrated to generate potential drops down to the innermost one. The entrance window is biased separately with respect to the detector back side allowing for an effective charge collection. There are guard cathodes that scale down the bias voltage to ground, both on the back and the front sides, outside the sensitive area of the whole array of cells. The readout anodes are wire bonded to ultra-low noise SIRIO charge sensitive preamplifiers on the front-end board. The SIRIO preamplifier developed by Politecnico di Milano is designed for SDDs readout in CMOS technology. It has intrinsic minimum noise levels of 1.27 and 1.0 electrons r.m.s. at +22 and −30 °C, which correspond to line's FWHM of about 11 eV and 8 eV, respectively, referring to silicon detectors [2]. This performance represents the current state of the art in low-noise front-end electronics for SDDs and the final energy resolution is practically determined by the detector anode dark current and by the parasitic capacitance of the preamplifier-detector connection. A threshold of the noise of only 5.6 electrons, corresponding to an energy of 21 eV, is obtained before connecting the preamplifier input to the detector anode. It increases up to 165 eV, corresponding to 45 electrons, if the SIRIO is connected to the anode of a 13 mm^2 SDD operating at room temperature [2]. SIRIO has a power consumption of about 10 mW including the output buffer.

2. – Two detector prototypes towards the final version

Two different prototypes have been built and tested at Elettra Synchrotron in Trieste. The first one (see fig. 2) has a front-end electronics that integrates the signal charge and performs an antialiasing filtering on the analog signal by means of a low-pass filter. The back-end, developed by Elettra Electronics Laboratory, has a 12 bit 8-channel ADC capable of encoding at 40 Msps. Data are digitally filtered with a set of suitable digital filters (not yet optimized at the date of the beamline test in September 2015) and analysed by an FPGA, which also handles the near-saturation reset of the preamplifiers. The reset of the preamplifiers is simultaneous for all channels and it is triggered by the first one reaching the near-saturation threshold. Data are transmitted over a TCP / IP connection to a PC running a dedicated LabVIEW software. The front-end electronics hosts also a shift register controlled by the FPGA that allows to hold each one of the eight channels in a reset state to let them disabled. Due to the light sensitivity of the sensor a small plastic case encloses the SDD, hence keeping it in a dark environment. Its entrance window comprises a stack of two alumined Mylar foils 25 μm thick.

A beam test was carried out at the XAFS beamline of Elettra in September 2015 with this prototype detector [3]. We demonstrated the capability to sustain a count rate up to 10^5 counts s^{-1} $cell^{-1}$ at the Mn fluorescence ($K\alpha$ at 5.89 keV, $K\alpha$ at 6.49 keV) with 18% of pile-up and a count rate of $5{\times}10^4$ counts s^{-1} $cell^{-1}$ with 9% of pile-up, considering an event acquisition dead time of 2 μs, showing that fluxes of the order of few 10^6 photons s^{-1} cm^{-2} are manageable.

A second prototype detector was built to test the actual front-end electronics chain for a single channel and the architecture of the digital filter based on the Finite Impulse Response (FIR) class (see top of fig. 3). FIR filters flexibility allows to constrain the filter synthesis by taking into account for the input signal noise, the optimization of the output shape (duration, flat top, symmetry), the rejection of low frequency pedestal variations and the minimization of the ADC quantization noise. The analog signal undergoes a pre-shaping analog filtering (CR-RC^2) with a peaking time of 500 ns and then it is passed as a differential pulse to the back-end electronics. A voltage comparator drives the trigger of

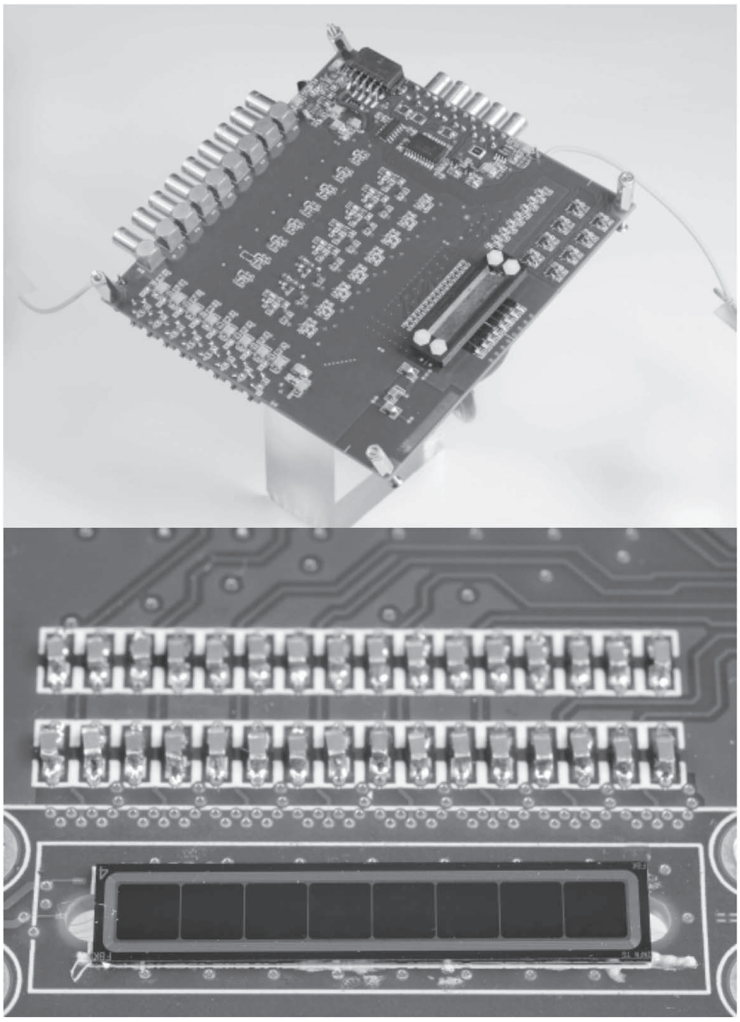

Fig. 2. – On the top the PCB of the first 8-channel prototype detector. The SDD is in the black plastic case with the alumined Mylar window. On the bottom the SDD mounted on the PCB.

the FPGA to reset the preamplifier when it is near saturation. The back-end electronics is adapted to handle differential signals with respect to the first detector prototype. In September 2016 this detector prototype was tested at the XAFS beamline of Elettra (see the bottom left of fig. 3). The SDD was Peltier cooled at +6 °C, thus to obtain a leakage current of 5 pA. The best energy resolution in terms of FWHM obtained at the 5.89 keV of the Mn $K\alpha$ line was 147 eV for 2.93×10^3 counts s^{-1} with negligible pile-up and a peaking time of about 1 μs (see the bottom right of fig. 3). No radiation collimation was used, therefore an improvement of the energy resolution is possible. The higher count rate verified was about 2.8×10^5 counts s^{-1} with a peaking time of about 1 μs and an energy resolution of 162 eV. No pile-up rejection algorithms were applied, resulting in a pile-up event fraction of about 34%.

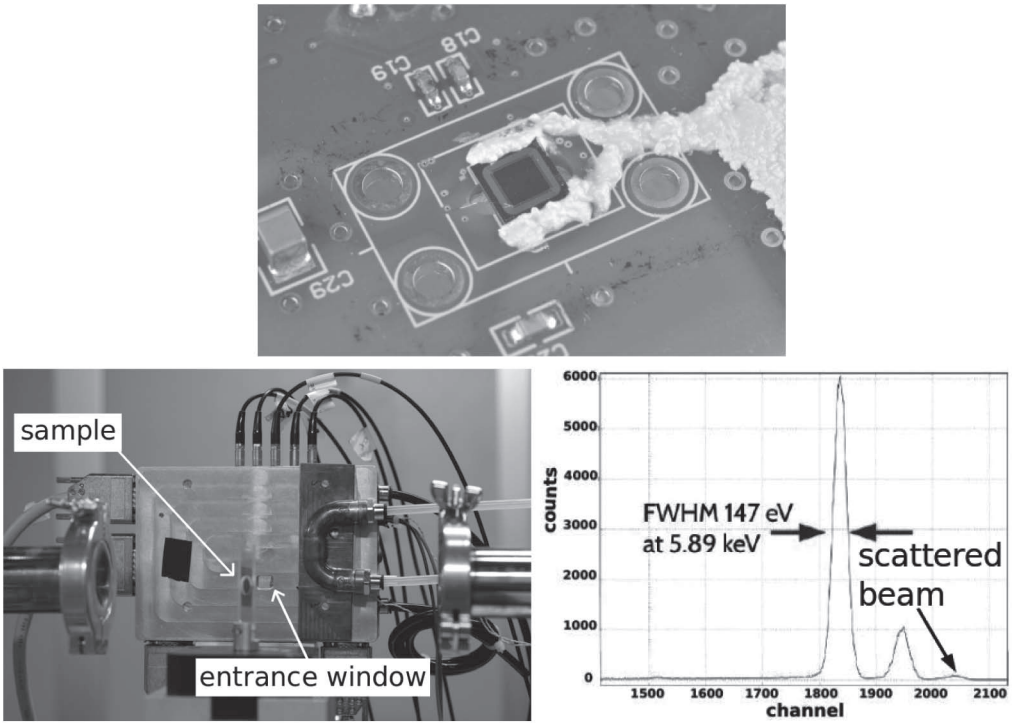

Fig. 3. – On the top the single-cell SDD mounted on the second detector prototype PCB. The cold side of a Peltier was in contact with the thermal conducting glue used to fix the SDD on the PCB. The hot side of the Peltier was in contact with the aluminum shielding case of the detector cooled by a water circuit at 20 °C. On the bottom left the test beam set-up of September 2016. On the bottom right the energy spectrum from a Mn foil. The energy resolution of the $K\alpha$ line in terms of FWHM is 147 eV at +6 °C with a peaking time of about 1 μs.

3. – The final detector design

In the final detector design the front-end electronics comprises two orthogonal PCBs mounted at 90° (see the top of fig. 4). The detector head dimensions are precisely calculated to fit the 8 cell SDD array, the preamplifiers, the connectors to the second front-end PCB and a minimal mechanical support. On the rear a Peltier cell is glued to a mechanical structure that allows to contact the detector head PCB and to cool the SDD. The heat from the hot side of the Peltier is removed by a water-filled heat pipe system and transferred out of the detector case to a water circuit at 20 °C. More detector heads (up to 8 in the current design) can be stacked with minimal dead spaces to have a larger collection area (see bottom of fig. 4). Each SDD has on-board thermistors for temperature control and a tungsten collimator in front of them allows to minimize "split" events between two cells, improving the energy resolution. A new SIRIO preamplifier, optimized for this detector, is now under test at Politecnico di Milano.

The second front-end PCB hosts the remaining electronics (fast analog shaping filter, input for the reset trigger to the FPGA, differentiation of the signal). The front-end modules are placed in a sealed case filled with a dry atmosphere to allow cooling down to −10° while preventing water condensation.

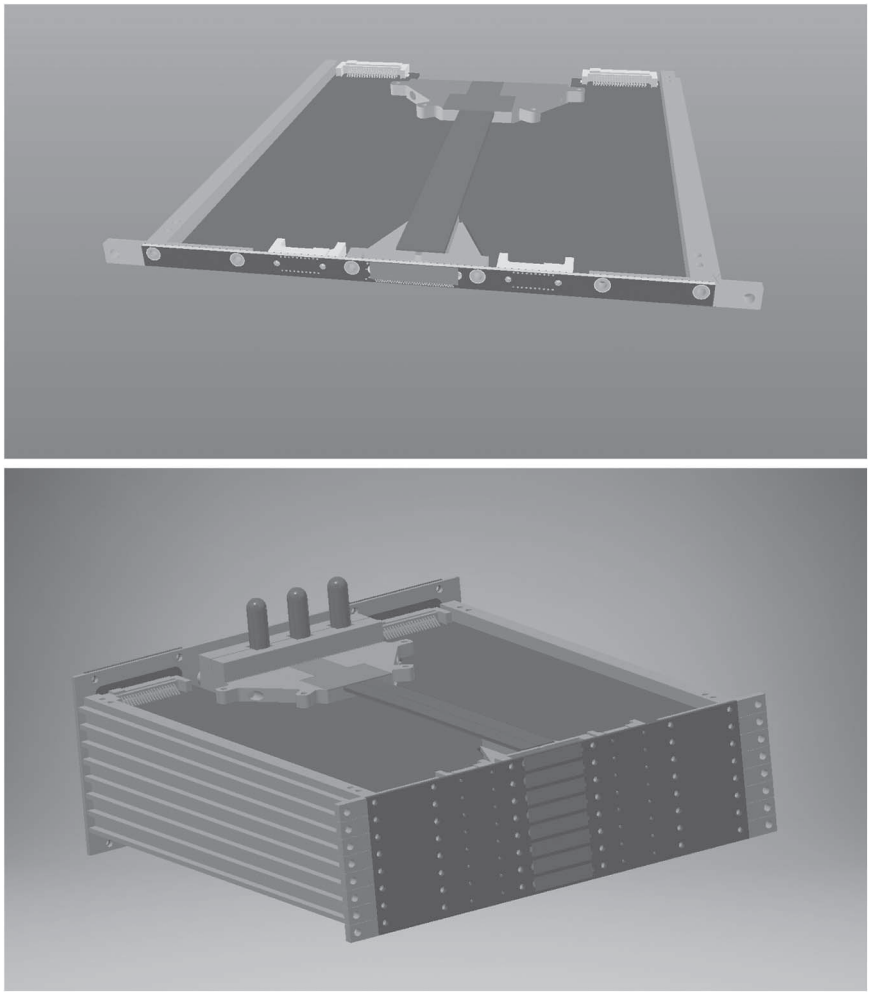

Fig. 4. – On the top the concept design of the final detector head. On the bottom the stacking of 8 front-end electronics PCBs.

The back-end electronics, directly connected to the front-end allows the configuration of the instrument, the digitization and elaboration of the analog signals, the acquisition of histograms or raw data for system analysis, the communication with the controlling computer. Depending on the conditioning circuit bandwidth it can allow for shaper rise times as fast as 250 ns. Noise filtering is accomplished by means of a low-power, high-performance ALTERA Cyclone 5 FPGA, which implements also the data buffers and the configuration and control logic. It features an Ethernet port (possibly in a separated board) for network communication with a host computer.

4. – Conclusions

The XAFS fluorescence detector under development is a state-of-the-art instrument. It will sustain a count rate of at least 5×10^4 counts s^{-1} $cell^{-1}$ ($\sim 5.6\times10^5$ counts $cm^{-2}\,s^{-1}$). The detector will have a total sensitive area of 576 mm^2 allowing for a total count rate

of at least 3.2×10^6 counts s^{-1} with an energy resolution $\leq$150 eV in terms of FWHM at 5.9 keV at 0 °C with a peaking time $\leq 1\,\mu$s. We verified experimentally that the prototype detector is already compliant to such requirements. It was moreover operated at the higher count rate of 2.8×10^5 counts s^{-1} $cell^{-1}$, corresponding to a total count rate of 1.8×10^7 counts s^{-1} for the 64 cells with only a small worsening of the energy resolution, but without applying any pile-up rejection algorithm.

The detector concept is being tested and optimized by way of two parallel developments for Elettra Synchrotron (XAFS and TwinMic beamlines) with good results. The time-frame set for this project forced us to consider conservative solutions, nonetheless further optimizations and improvements of such detector are possible and will be pursued in future developments.

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REFERENCES

[1] Geant4 Collaboration, *Geant4: A Simulation Toolkit for the Passage of Particles through Matter, Astrophysics Source Code Library* (2010).

[2] Bertuccio G., Ahangarianabhari M., Graziani C., Macera D., Shi Y., Gandola M., Rachevski A., Rashevskaya I., Vacchi A., Zampa G., Zampa N., Bellutti P., Giacomini G., Picciotto A., Piemonte C. and Zorzi N., *IEEE Trans. Nucl. Sci.*, **63** (2016) 400.

[3] Fabiani S., Ahangarianabhari M., Baldazzi G., Bellutti P., Bertuccio G., Bruschi M., Bufon J., Carrato S., Castoldi A., Cautero G., Ciano S., Cicuttin A., Crespo M. L., Dos Santos M., Gandola M., Giacomini G., Giuressi D., Guazzoni C., Menk R. H., Niemela J., Olivi L., Picciotto A., Piemonte C., Rashevskaya I., Rachevski A., Rignanese L. P., Sbrizzi A., Schillani S., Vacchi A., Villaverde Garcia V., Zampa G., Zampa N. and Zorzi N., *J. Phys. Conf. Ser.*, **689** (2016) 012017.