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CMOS pixel development for the ATLAS experiment at the High Luminosity LHC

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Summary. — To cope with the rate and radiation environment expected at the HL-LHC, new approaches are being developed on CMOS pixel detectors, providing charge collection in a depleted layer. They are based on: high-voltage enabling technologies that allow to use high depletion voltages, high-resistivity wafers for large depletion depths; radiation-hard processes that allow for CMOS electronics embedded into the sensor substrate. Since 2014, several groups in the ATLAS experiment are actively pursuing CMOS pixel R&D within an ATLAS Demonstrator program for sensor design and characterisations. The goal of this program is to demonstrate that depleted CMOS pixels, with monolithic or hybrid designs, are suited for high-rate, fast timing and high-radiation operation at LHC. For this, a number of technologies have been explored and characterised.

1. – Introduction

The high luminosity upgrade of the Large Hadron Collider (HL-LHC) aims to bring the LHC peak luminosity from the design value of $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ to $5\text{–}7\times10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ [1]. The tracking system of the ATLAS experiment is being re-designed to cope with a particle rate of 1 GHz/cm^2 in the innermost layers, sustaining a dose of 1 Grad and a non-ionising energy loss (NIEL) equivalent to the one induced by 10^{16} 1 MeV neutrons per cm^2 (n_{eq}/cm^2) [2]. Improved detector technologies and front-end electronics are needed to achieve these requirements.

Silicon pixel detectors built in commercial CMOS processes are a possible solution to this challenge. CMOS monolithic active pixels (MAPS) have already been deployed in heavy ion experiments [3, 4] and are an option for future high energy lepton colliders [5]. In these detectors, the collection of the ionisation signal proceeds mainly by diffusion of the charge carriers. The corresponding long collection time makes them unsuitable for operation at the HL-LHC, due to the required time resolution of 25 ns and the short carrier lifetime due to radiation damage. CMOS detectors coupled with a depletion

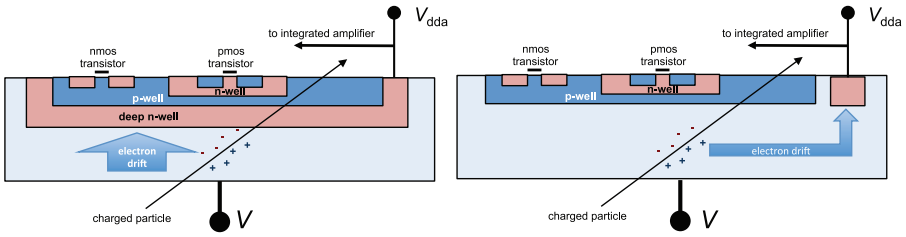

Fig. 1. – Sketches of the two main options for HV/HR-CMOS pixel designs, on the left the large fill factor, and on the right side the small fill factor.

layer [6] may overcome the limitation of standard MAPS by collecting carriers by drifting them in the depleted region, and they are the subject of active investigation to assess their radiation hardness and rate capability.

2. – Technologies and sensor designs

The size d of the depleted region of a planar silicon sensor depends on the silicon dielectric constant, $\varepsilon_{\mathrm{Si}} \approx 1\,\mathrm{pF/cm}$, the charge carrier mobility μ, the bulk material resistivity ρ, the built-in potential V_{bi}, and the applied bias V, according to the relationship $d = \sqrt{2\varepsilon_{\mathrm{Si}}\mu\rho(V + V_{\mathrm{bi}})}$ [7]. The key enabling technologies for the construction of depleted CMOS sensors are processes allowing to sustain V in the range from several volts to hundreds of volts (HV-CMOS, often driven by the requirements of automotive or power application), in which custom substrates with moderately high resistivity, $\rho = 10\text{–}10000\,\Omega\cdot\mathrm{cm}$, can be used (HR-CMOS). They are now available from several manufacturers, with feature sizes in the 130–180 nm range.

Detectors with this technologies can be built in two major configurations. The "large fill factor" design, illustrated in the left panel of fig. 1, uses a deep n-well or a buried layer as a collecting electrode and integrates the front-end electronics inside this well. It provides a short drift path and uniform charge collection efficiency, at the cost of a diode capacitance C_{det} of the order of 100 fF, dominated by the parasitic capacitance to the internal p-well. The "small fill factor" design is shown in the right panel of fig. 1. It is characterized by a small size collecting electrode, with C_{det} of few fF, and front-end electronics built outside the electrode. The small input capacitance is beneficial to the noise, $\propto C_{\mathrm{det}}$, and to the risetime, $\propto 1/C_{\mathrm{det}}$ [7]. The drawback is the non-uniformity of the drift field, with longer drift paths, depending on the particle crossing point, and therefore larger trapping probability after irradiation.

3. – Sensor performance

Depleted CMOS detectors have been realized in different technologies by institutes collaborating to the R&D for the upgrade of the ATLAS Inner Tracker (ITk) for the HL-LHC. They have been characterized, before and after irradiation, with laboratory setups and test beams. Figure 2 shows some significant results.

In fig. 2(a), the size of the depleted region *vs.* the bias voltage is shown for a large fill factor CMOS sensor (CCPD-LF [8]) realized with the LFoundry 150 nm process on a high-resistivity substrate ($\rho > 2\,\mathrm{k\Omega\cdot cm}$) [9]. The measurements are obtained with the edge transition current technique (E-TCT). The different lines correspond to devices

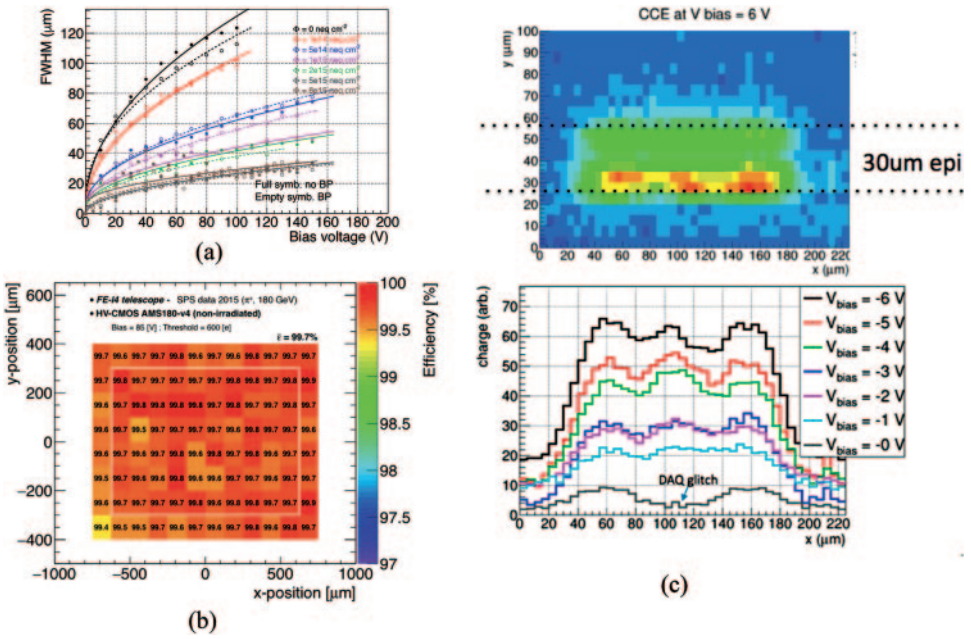

Fig. 2. – Selected results from depleted CMOS sensor prototypes: (a) E-TCT measurement of the depletion depth *vs.* V for LFoundry large fill factor sensors irradiated at different doses [8]; (b) test beam efficiency for large fill factor sensors in the AMS H18 process [11]; (c) E-TCT measurement of charge collection efficiency as a function of the position for an array of three small fill factor pixels in a TowerJazz process, irradiated at 10^{15} $n_{\mathrm{eq}}/\mathrm{cm}^2$: the top figure shows the charge collection as a function of the depth y inside the sensor, the bottom figure is a slice at $y = 30\,\mu$m [14].

irradiated with neutrons up to a fluence of 5×10^{15} $n_{\mathrm{eq}}/\mathrm{cm}^2$, with or without backside processing (BP) for thinning and providing an ohmic contact to the substrate. Even after large doses, a sizable depleted region can be achieved at moderate bias voltage, providing a detectable signal. The efficiency of a small matrix of $50 \times 250\,\mu\mathrm{m}^2$ pixels coupled to a FE-I4 chip [10] is shown in fig. 2(b). These pixels implement a large fill factor design in the AMS 180 nm HV technology. The observed efficiency is 99.7% before irradiation, and is constant up to a fluence of 10^{15} $n_{\mathrm{eq}}/\mathrm{cm}^2$ [11].

The charge collection efficiency has also been studied for a small fill factor design, implemented in the Investigator chip [12] in the TowerJazz 180 nm process. As an example, an array of three $50 \times 50\,\mu\mathrm{m}^2$ pixels, implanted on a $30\,\mu$m thick epitaxial substrate, is shown in fig. 2(c). The collected charge from the laser pulse of the E-TCT, as a function of the injection point, for this device, irradiated to 10^{15} $n_{\mathrm{eq}}/\mathrm{cm}^2$, displays a good uniformity, providing a detectable signal even with biases in the few-volt range [13].

The observed results are very encouraging and point to the fact that radiation hard CMOS sensors for operation at the HL-LHC are technically feasible.

4. – Readout architectures

For operation in an experiment, a radiation hard depleted CMOS sensor must be integrated with a readout architecture able to perform a sparse readout and to transmit data to the off-detector data acquisition system.

For a very high particle rate, a possible solution is the hybridisation of the CMOS sensor to the front-ends chips under development within the RD53 Collaboration for the readout of pixel detectors at the HL-LHC [15]. This can be achieved either by bump-bonding or by capacitive coupling via a thin dielectric adhesive layer (capacitive coupled pixel detector, CCPD) [16].

Another solution is a fully monolithic design, integrating in the same chip both the sensor and readout components. It has the significant advantages of simplifying the detector construction and of reducing the material budget, since no additional front-end chip is needed. The HV/HR CMOS technologies have features sizes larger than the 65 nm of the TSMC technology adopted by RD53, anyhow, their level of integration is comparable to the 130 nm IBM process used for the FE-I4 [10], and it should allow for the implementation of a readout architecture managing a data rate corresponding to a particle flux of 0.1 GHz/cm^2, as foreseen in the outermost pixel layers.

Prototypes are being developed in the same CMOS processes discussed in sect. **3**. Different architectures are under investigation. Direct transfer of analog hit information from the pixel cells to the chip periphery has minimal power consumption and does not require distribution of clock and trigger information along the pixel matrix, reducing cross talk between the analog signal processing and the digital readout. Alternative approaches are a column-drain readout, as implemented in the ATLAS FE-I3 chip [17], or a readout based on a block of pixels, similar to the FE-I4 or RD53 architectures [10, 15]. These solutions must be verified in term of sensitivity to noise and cross-talk, and of data rate capability on the first lots of monolithic CMOS devices currently under manufacturing.

5. – Conclusions

Depleted CMOS sensors are undergoing an active R&D phase. Significant progresses have been achieved on the CMOS sensors, observing efficiencies better than 99% after irradiation at fluences greater than 10^{15} n_{eq}/cm^2. Recently very encouraging results have been shown for small fill factor designs: this is very attractive because of their low input capacitance and low power.

The next step is the integration of the sensors with a high rate readout architecture. For extremely high rates, a hybrid solution, with capacitive coupling to a highly integrate front-end electronics is under development. The currently used sensor technologies, with their 130–180 nm feature size, should allow the realisation of monolithic solutions able to sustain the hit rate of the external pixel layers at the HL-LHC and some prototypes are being produced.

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