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Readout upgrade for the ATLAS Pixel Detector: Reasons, status and results

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Summary. — This work intends to briefly overview the readout upgrade for the ATLAS Pixel Detector. Two electronic boards compose the readout chain: Back Of Crate and ReadOut Driver. The two boards were designed to interface the chip FEI4, the front-end chip used in Insertable B-Layer, the innermost and most recent layer of the ATLAS Pixel Detector. Due to the characterizing low latency, high bandwidth and system versability, those boards achieved exceptional results and were chosen to replace the readout electronic of Layer 2, Layer 1, the B-Layer and the Disks. In this work the reasons for the ATLAS Pixel Detector readout upgrade will be discussed, as well as the technological solution adopted and the achieved results.

1. – Introduction

The Large Hadron Collider (LHC) was designed to reach an energy of 14 TeV in the center of momentum frame of pp collisions and an instantaneous luminosity of $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, which has already been reached during Summer 2016. LHC is planning, in the short term, to further enhance the luminosity, resulting in an increased pileup and a higher trigger frequency. These factors constitute a challenge for the data readout since the amount of data to be transmitted per time unit depends on both pileup and trigger frequency. In the ATLAS experiment, the data-taking is particularly challenging for the Pixel Detector, which is the detector closest to the beam pipe. In order to face these experimental challenges, the readout system has been upgraded during the last few years for each layer of the Pixel Detector: IBL (2015), Layer 2 (2015–2016), Layer 1 (2016–2017) and B-Layer (2017–2018) [1]. The main purpose of the upgrade was to provide a higher bandwidth by exploiting recent technologies. The new readout system is composed by two paired electronic boards, Back Of Crate (BOC) and ReadOut Driver (ROD) that replaced the previously installed Silicon BOC (SiBOC) and Silicon ROD (SiROD).

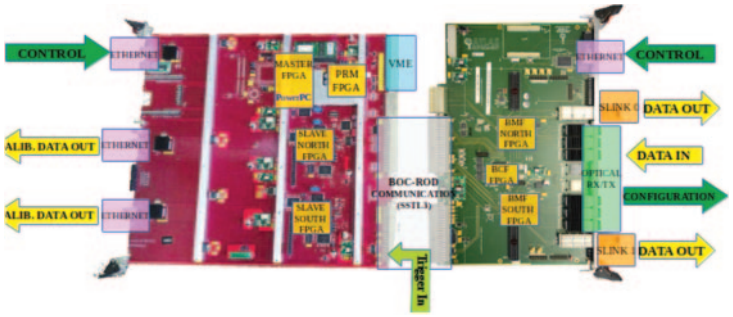

Fig. 1. – Part of the ATLAS Pixel Detector readout chain. The ROD board (on the left) features 3 Spartan-6 FPGAs (PRM, Slave North and Slave South) and one Virtex-5 FPGA (Master). The BOC board (on the right) features 3 Spartan-6 FPGAs (BCF, BMF North and BMF South). The input-output connections are also shown in the figure.

2. – ATLAS Pixel Detector readout overview

The ATLAS Insertable B-Layer (IBL) [2] and Pixel Detector readout chain is composed by several components. The front-end chips, front-end readout chip FEI4 [3] for IBL or FEI3 and Module Chip Controller (MCC) [4] for the other pixel layers, are bonded to the detector and send data via optical fiber to the readout electronics, sited 100 m far from the detector. The readout electronics is composed by two boards: BOC, responsible for handling the control interface to the detector and the data from the detector and for providing the clock to the connected detector parts, and ROD, a VME board which processes data and sends commands to the front-end modules. The two boards are also shown in fig. 1. Another main component of the readout chain is the Timimg and Trigger Control (TTC) Interface Module (TIM), which interfaces the ATLAS Level-1 Trigger system signals to Pixel subdetectors.

3. – Results

The primary reason for the readout chain upgrade is the ability to handle a high occupancy and a high trigger rate. A lower bandwidth would lead to link saturation, causing loss of important physical data. The most problematic layers in terms of link saturation were Layer 2 and Layer 1; the upgraded system solved the problem by doubling the readout speed. Hence, it proved able to cope with the amount of data produced by

TABLE I. – *Comparison between old and new readout system. B-Layer data not available yet.*

Layer	Readout Speed per link (old/new)	Link occupancy at $\mu = 60$ (old/new)
IBL	−/160 Mbps	−/50%
B-Layer & Disks	160/160 Mbps	81/−%
Layer 1	80/160 Mbps	103/52%
Layer 2	40/80 Mbps	159/79%

LHC so far. Furthermore, it is highly configurable and provides many monitoring tools, resulting in the capability of quickly identifying and solving problems. Table I shows a comparison between the old and the new readout system in terms of readout speed and link occupancy.

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