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The upgrade of the Inner Tracking System of the ALICE experiment

I. RAVASENGA(1)(2) on behalf of the ALICE COLLABORATION

(1) *Dipartimento DISAT del Politecnico di Torino - Turin, Italy*
(2) *INFN, Sezione di Torino - Turin, Italy*

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Summary. — In 2021, for the third run of the CERN Large Hadron Collider (LHC), Pb-Pb collisions will be performed at a centre-of-mass energy per nucleon of 5.5 TeV, with an integrated luminosity of $6 \times 10^{27}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and at an unprecedented interaction rate up to 50 kHz. To fulfil the requirements of the ALICE physics program for Run 3, the ALICE experiment at LHC is planning a major upgrade during the Long Shutdown 2 of LHC in 2019–2020. One of the key elements, is the construction of a new ultra-light and high-resolution Inner Tracking System (ITS) to enhance the determination of the distance of closest approach to the primary vertex, the tracking efficiency at low transverse momenta, and the read-out rate capabilities, with respect to what can be achieved with the current detector. It will consist of seven layers equipped with silicon Monolithic Active Pixel Sensors (MAPS) with a pixel size of the order of $30 \times 30\,\mu\mathrm{m}^2$ built with the Towerjazz $0.18\,\mu$m CMOS Imaging process.

1. – Physics motivation

The ALICE Collaboration at the CERN Large Hadron Collider (LHC) is building a major upgrade of the experimental apparatus to be installed during the Long Shutdown 2 of LHC in 2019–2020. The upgrade aims at enhancing the physics capabilities of ALICE for the measurements of rare probes on a wide range of transverse momenta in pp, p-Pb and Pb-Pb collisions. The physics goal consists in reaching high-precision measurements of the Quark-Gluon Plasma (QGP) state, studying heavy-flavour quarkonia down to very low p_T, vector mesons and low-mass dileptons, as well as light nuclei and hyper-nuclei.

The upgrade of the ALICE Inner Tracking System (ITS) plays a key role for the enhancement of the physics capabilities relaying on the determination of the distance of closest approach to the primary vertex, the tracking efficiency at low transverse momenta ($< 1\,\mathrm{GeV}/c$), and the read-out rate [1, 2].

TABLE I. – *Main technological features of updraded ITS compared to the present ITS.*

	Present ITS	Upgraded ITS
Readout rate	up to 1 kHz	> 100 kHz (Pb-Pb) > 400 kHz (pp)
Material budget	1.1% X_0	0.3% X_0 (Inner Barrel) $\sim$1% X_0 (Outer Barrel)
Pixel size	$50 \times 425\,\mu\text{m}^2$	$\mathcal{O}\,(30 \times 30\,\mu\text{m}^2)$
Resolution ($p_T = 500\,\text{MeV}/c$)	$\sim$240 μm (z) $\sim$120 μm ($r\varphi$)	improvement by a factor 5 (z) 3 ($r\varphi$)

2. – The upgrade of the ALICE ITS

The upgraded ITS will be equipped with seven cylindrical and concentric layers of silicon Monolithic Active Pixel Sensors (MAPS) called ALPIDE (ALice PIxel DEtector) reaching a total active area of about $10\,\text{m}^2$ and a pseudo-rapidity acceptance $|\eta| < 1.22$. The main features of the upgraded ITS compared to the ones of the present detector are summarised in table I [1].

The sensors, produced by Towerjazz with its $0.18\,\mu$m CMOS Imaging process, have a pixel dimension of $\sim 27 \times 29\,\mu\text{m}^2$. The main features of ALPIDE are 1) a n-well diode about 100 times smaller than the pixel, leading to a small capacitance of few fF; 2) a fast data-driven encoder [5] with an integration time of $\sim 2\,\mu$s and, 3) a n-well of p-MOS transistors shielded by a deep p-well permitting a full CMOS circuitry within the active volume [3, 4]. The detection efficiency and the fake-hit rate of irradiated and non-irradiated ALPIDE chips were measured in various beam tests demonstrating a sufficient operational margin even after 10× lifetime Non-Ionizing Energy Loss (NIEL) dose (see fig. 1).

The ALPIDE chips are arranged in rectangular structures called Modules. A Flexible Printed Circuit (FPC) wire-bonded to the chips in a Module is used for clock, control and data transmission towards and from the outside electronics [1]. The Modules were tested in laboratory measuring a robustness to tens of thermal cycles in a temperature range from about 10 °C up to 60 °C.

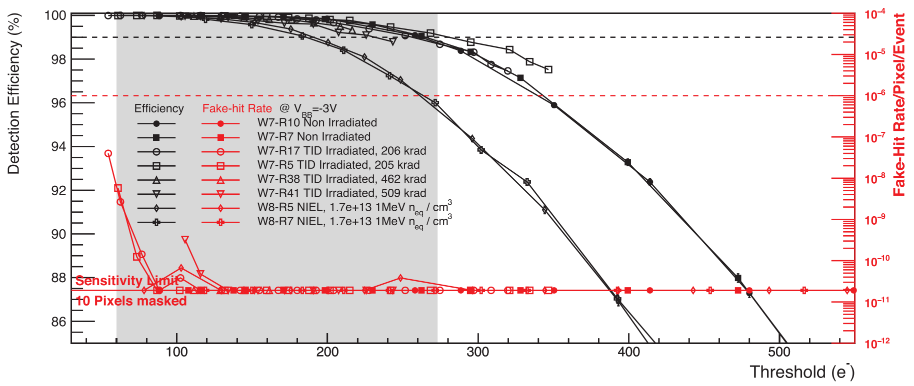

Fig. 1. – Efficiency and fake-hit rate as a function of the threshold for irradiated and non-irradiated chips measured at the CERN Proton Synchrotron with $6\,\text{GeV}/c^2$ pions.

Finally, the longitudinal Staves host the Modules, the FPCs, a Cold-Plate for chip cooling and a Power-Bus for chip powering. The OB Stave is then formed by two independent Half-Staves. An ultra-light carbon-fiber Space Frame supports the detectors and all the circuitry.

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