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# Versatile multi-channel CMOS frontend with selectable full-scale dynamics from 100 MeV up to 2.2 GeV for the readout of detector's signals in nuclear physics experiments

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**Summary.** — We developed a versatile multichannel CMOS frontend with selectable full-scale energy range from 100 MeV up to 2.2 GeV for the readout of detector's signals in nuclear physics experiments. The core of the frontend electronics is a custom designed CMOS charge preamplifier able to guarantee an energy resolution of the order of 10 keV FWHM with a power budget of about 10 mW/channel (ASIC only). 16-channel charge preamplifiers are integrated in a single chip in ams 0.35 $\mu$m C35B4C3 technology together with the CsI(Tl) frontend and few additional slow control services. A dedicated 8 layer frontend motherboard houses 2 ASICs and the line-drivers needed to provide a differential output and to drive the several-meter long connections. High-density right-angle open-pin-field connectors interconnect the motherboards and a patch-panel responsible of the slow-control and the interconnections to the meters-long cables. The designed frontend is extremely versatile, being suitable to be coupled to different detector topologies and signal polarities with capacitances ranging from about 10 pF up to about 200 pF. The first application of the developed frontend is to instrument the FARCOS (Femtoscope ARray for Correlation and Spectroscopy) detection system, a novel detector featuring high angular and energy resolution able to reconstruct the particle's momentum at high precision and capable of performing correlation measurements of LCPs and of LCPs and IMFs. A thorough experimental qualification allowed verifying the frontend performance. The measured energy resolution with the frontend coupled with a 300 $\mu$m thick Double Sided Silicon Strip Detector (DSSSD) of the FARCOS telescope illuminated with a mixed-nuclei $\alpha$ source shows a resolution below 10 keV FWHM. The paper focuses on the designed frontend system and on the results of its qualification.

## 1. – Motivation of the work

With the advent of radioactive beams, the nuclear physics community is active in developing novel experimental methods and instruments coping with beam characteristics to extract spectroscopic information and study novel nuclear reaction mechanisms [1, 2].

 

Nowadays, nuclear particle physics instrumentation require a full cover of the available phase space with good efficiency, angular, energy and particle identification capabilities. From the detector standpoint this fact pushes towards the use of multi-channel detectors with moderately fine pitches. In addition different types of detectors in very close geometry around the target are required, often operating in vacuum. Therefore multichannel, low-power, compact readout electronics is mandatory, pushing towards the integration of the frontend electronics in CMOS technology. The tendency is towards Digital Pulse Shape Acquisition, a powerful technique that opens the way to fully exploit the information encoded in the detector output response. The resolution in charge and mass separation and the energy threshold achievable with a chosen pulse-shape processing technique are strictly related to the physical properties and to the topology of the detector, to the experimental setup (*i.e.*, front-side or reverse-side mounting) as well as to the type (*i.e.*, charge-sensing or current-sensing) and performance of the analogue frontend [3]. The key feature to preserve the fast rise time of the preamplifier output and the signal integrity over meters-long connections from inside the vacuum chamber to the backend electronics is to feed a differential output to shielded differential pairs. The peculiarity of the ample dynamic range and integral-non-linearity normally required in nuclear physics experiments impose careful design and extended experimental qualification not to spoil performance with respect to conventional electronics.

The paper is organized as follows. Section **2** describes the designed frontend; sect. **3** illustrates the results of the experimental qualification and sect. **4** ends with conclusions.

## 2. – The designed frontend

The guideline for the design of a versatile frontend for the readout of detector's signals in nuclear physics experiments is the one design "fits-all" philosophy, so that the same design can be used to readout signals of both polarities coming from a large variety of detectors with output capacitance in the range 10 pF–200 pF while preserving the paradigm that the detector and the frontend electronics have to be considered an inseparable pair. In this way spare management becomes easy and costs reduced. The designed frontend has to be suitable for pulse shape technique, therefore the designed frontend amplifies the whole signal waveform without amplitude and shape distortion. The ASIC provides digitally selectable full-scale energy ranges at 0.5% $INL$ of 100 MeV, 250 MeV, 400 MeV, 550 MeV and 2.2 GeV to cope with different experimental requirements. The target static power consumption is about 10 mW/channel. Single-channel ASIC or multi-channel ASIC of 8 or 16 channels are available to cope with different detector types. The zero-capacitance 20%–80% rise time below 10 ns allows coping even with fast charge collection times.

**2**˙1. *Architecture of the designed ASIC*. – The frontend is based on a charge preamplifier configuration, DC coupled or AC coupled, with an external capacitor and biasing resistor [4-6]. Figure 1 shows the simplified schematics of the charge sensitive preamplifier in CMOS ams C35B4C3 technology. The preamplifier features a continuous-reset feedback and an input PMOS transistor in telescopic cascode configuration. Two options are available for the feedback, an integrated PMOS with aspect ratio suitable to work in the ohmic region and an external feedback resistor. Independent biasing of the first branch allows a single chip to readout both signal polarities. The power dissipation is limited to $\leq$10 mW/channel, therefore the first transistor operates in moderate-weak inversion.

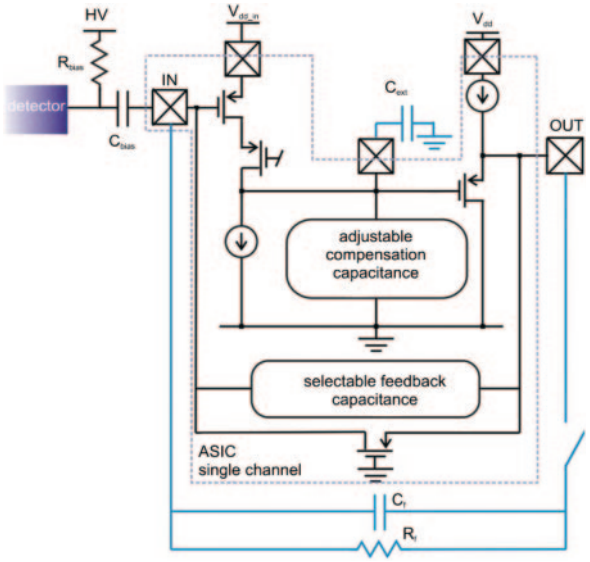


Fig. 1. – Simplified schematics of the charge sensitive preamplifier. The circuit in the box is produced in ams CMOS C35B4C3 technology. The external SMD feedback capacitance ($C_f$) and resistance ($R_f$) are activated thanks to a low-capacitance, low-resistance analogue switch.

The chosen technology (ams $CMOS\ C35B4C3$) features 3.3 V supply voltage, 0.35 $\mu$m minimum feature size, 4 metal layers, high resistivity poly and poly precision capacitors. A complete stand-alone channel is 1000 $\mu$m wide and 370 $\mu$m long, including all needed services. The designed preamplifier can be used to assemble multi-channel chips, at present up to 16-channel ASICs have been designed and tested with an occupied area that can be as low as 5270 $\mu$m $\times$ 1000 $\mu$m. Each chip foresees additional services, like an on-chip pulser, a channel-by-channel test signal injection system and a temperature monitor.

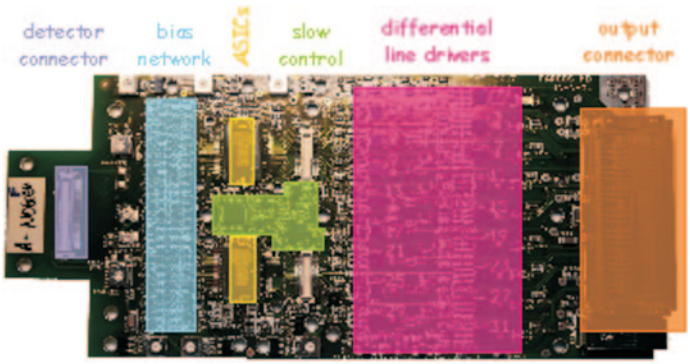


Fig. 2. – Photograph of the custom designed 8-layer PCB that houses two (16 + 1)-channel ASICs and reads out 32 + 2 detector channels.

**2˙2.** *Frontend board.* – Figure 2 shows the photograph of the custom designed 8-layer PCB that houses two $(16 + 1)$-channel ASICs and reads out $32 + 2$ detector channels (*e.g.*, one DSSSD side and one/two CsI(Tl) in the case of a detector telescope arrangement). Differential line drivers drive the signals coming from the ASIC towards the output of the vacuum chamber through 10 meter-long cables. Hi-Density right-angle open-pin-field connectors (Samtec $SEAF$-30-01-L-06-1-$RA$-$TR$) interconnect the motherboard with the slow control board. Other input/output connectors are possible. A dedicated calibration circuitry is placed on the frontend board in order to ease the debug and the calibration of the full system during mounting and data taking. The full calibration routine as well as the telescope slow control are handled by a microcontroller placed on the slow-control board. The ASIC supply voltages are generated locally on board to minimize disturbances.

**2˙3.** *Frontend slow control.* – The slow-control system is responsible of monitoring the ASIC and board temperature and setting all the ASIC control bits for proper configuration. In addition it provides the input test signals needed for system calibration according to a given pattern. The architecture of the slow control foresees a master microcontroller outside the vacuum chamber and communicating via $RS485$ (through opto-couplers) to the host PC and to each slow control board. The master microcontroller oversees the slow-control system, while the local cluster slow control is based on the microcontroller housed on the slow-control board. The microcontroller communicates via $I^2C$ to the DAC and the port expander present on each motherboard. All microcontrollers are in sleep mode during measurement to prevent pick-ups from the digital section. The port expander keeps the bit assignment when the microcontroller enters the sleep mode.

## 3. – ASIC experimental qualification

We fully characterized different versions of the chip standalone, with a detector-like input load capacitance and coupled with different detectors prototypes:

- 300 $\mu$m thick DSSSDs - BB7 design provided by Micron Semiconductor Ltd.
- 1500 $\mu$m thick DSSSDs - BB7 design provided by Micron Semiconductor Ltd.
- $1.8 \times 1.8\,\mathrm{cm}^2$, 300 $\mu$m thick silicon PIN diode provided by Hamamatsu ($S3204$-08), optically coupled with a $3.2 \times 3.2\,\mathrm{cm}^2$, 6 cm thick CsI(Tl) scintillator crystal
- $1\,\mathrm{cm}^2$, 300 $\mu$m thick silicon PIN diode provided by Hamamatsu ($S3590$-09)

Figure 3 shows the measured 20%–80% rise time as a function of the added input capacitance. The 20%–80% rise time keeps below 20 ns at 65 pF added input capacitance (mimicking the coupling with a 300 $\mu$m DSSSD-BB7 design). Up to 500 MeV full-scale energy range the rise time is below 20 ns with no slew rate limitation, at 2.2 GeV (on the falling edge) the rise time is below 30 ns, making the designed frontend a versatile option for input capacitances in the range 10 pF–220 pF. We assessed the integral-non-linearity via electrical injection and verified up to more than 500 MeV with a pulsed 3 MeV proton beam with variable bunch multiplicity (from 1 proton up to more than 200 protons) at the DeFEL beamline [7] of LaBeC [8], INFN, Firenze (Italy). For every input signal amplitude, the integral-non-linearity is computed as the maximum deviation from the linear $LSQ$ fit up to the considered amplitude. INL keeps below $\leq$0.5% over all the designed energy ranges for both signal polarities and all detector capacitances.

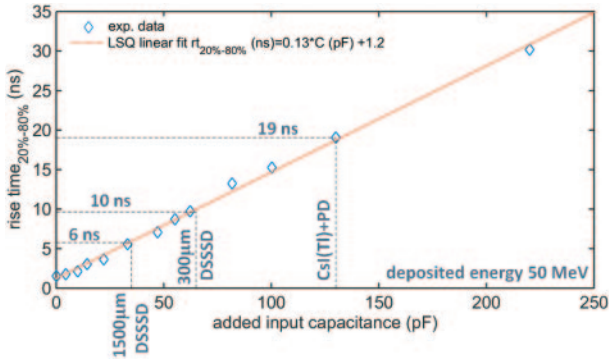


Fig. 3. – Measured 20%–80% rise time as a function of the added input capacitance. The capacitance level of the different tested detectors is highlighted.

We measured in the lab an energy resolution of 7.7 keV FWHM at the pulser line with the designed frontend coupled with a 300 $\mu$m thick DSSSD BB7 design (junction side strip, external resistor feedback, 100 MeV dynamic range). Figure 4 shows the spectrum measured at one channel (junction side strip, MOS feedback, 100 MeV full scale energy range) of a 300 $\mu$m thick DSSSD BB7 design irradiated with a mixed nuclei $\alpha$ source at the DeFEL beamline of LaBeC, INFN, Firenze (Italy). $4 \times 16$ channels ASICs were in operation. Figure 5 shows the measured energy resolution for the different full-scale energy ranges. The energy resolution measured with the designed frontend coupled with the *BB7* design 300 $\mu$m thick DSSSD is below 10 keV FWHM at 100 MeV full-scale energy range, below 15 keV FWHM at 500 MeV full-scale energy range and below 34 keV FWHM at 2.2 GeV full-scale energy range. The achieved energy resolution at the Cs-$K\alpha$ line is 7.8 keV FWHM when the designed frontend reads out a 1 cm$^2$ photodiode (Hamamatsu *S*3590-09) illuminated with a $^{133}$Ba source (5th order pseudo-Gaussian

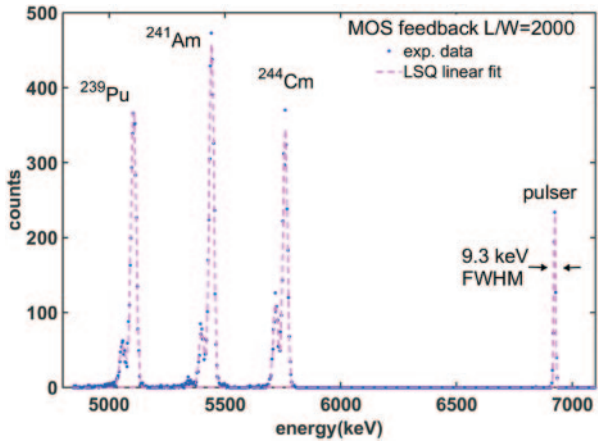


Fig. 4. – Measured spectrum at one channel (junction side strips, MOS feedback, 100 MeV full-scale energy range) of a 300 $\mu$m thick DSSSD BB7 design irradiated by a mixed nuclei $\alpha$ source at the DeFEL beamline of LaBeC, INFN, Firenze (Italy).

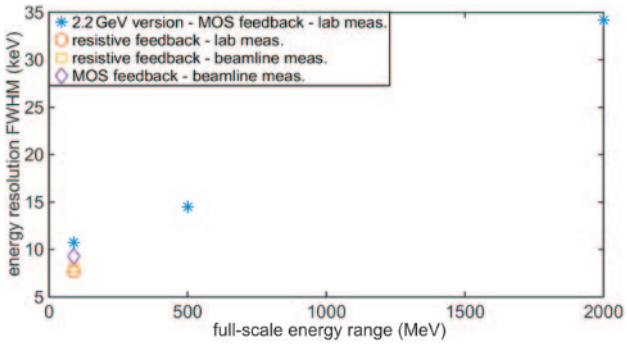


Fig. 5. – Measured energy resolution at the pulser line, as a function of the selected full-scale energy range in the case of a 300 $\mu$m thick DSSSD BB7 design.

shaper at 1 $\mu$s shaping time). The energy resolution measured in the lab at the $^{241}$Am $\alpha$ line detected by a CsI(Tl) scintillator 6 cm thick coupled with a 1.8 cm$\times$1.8 cm photodiode and readout with the designed frontend (external resistor feedback, 100 MeV dynamic range Si equivalent) is 179 keV FWHM.

## 4. – Conclusions and outlook

We developed a compact and versatile multichannel CMOS frontend with electronically selectable full-scale energy range from 100 MeV up to 2.2 GeV for the readout of detector's signals in nuclear physics experiments. A built-in pulser accounts for system debugging and calibration. A single ASIC design reads out signals of both polarities, from different detector types (pn diodes, DSSSDs of different thicknesses, scintillators coupled with photodiodes...) with output capacitances in the range 10 pF–220 pF. The measured 20%–80% rise time is below 20 ns up to 550 MeV full-scale energy range and keeps below 30 ns up to 2.2 GeV full-scale energy range. The measured INL is below 0.5% over the different full-scale energy ranges up to 2.2 GeV. The measured energy resolution (with the frontend coupled with a 300 $\mu$m thick DSSSD-BB7 design) is below 10 keV FWHM at 100 MeV full-scale energy range, below 15 keV FWHM at 500 MeV full-scale energy range and below 34 keV FWHM at 2.2 GeV full-scale energy range. The power consumption is below 10 mW/ch. We designed and successfully tested 32-channel frontend boards, now ready to use. The designed frontend will readout all the FARCOS [9] channels:

- DSSSD: (20 telescopes $\times$ 2 layers $\times$ 32 channels/side $\times$ 2 sides) = 2560 channels
- CsI(Tl): (20 telescopes $\times$ 4 CsI(Tl)) = 80 channels

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