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Development of the Experiment Control System for the LHCb RICH upgrade

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Summary. — This contribution presents the development of the Experiment Control System for the upgrade of the two ring-imaging Cherenkov detectors at the LHCb experiment, allowing to test and operate the Photon Detector Modules using the new architecture of the LHCb readout system. The RICH upgrade database, interfacing with the Experiment Control System, is also described.

1. – Introduction

The LHCb experiment [1, 2] is preparing for an upgrade during the second Large Hadron Collider (LHC) long shutdown in 2019–2020 [3]. In order to fully exploit the LHC flavour physics potential with a fivefold increase in the instantaneous luminosity, an entirely software trigger strategy will be implemented. The hardware trigger stage will be removed, and, therefore, all the LHCb subdetectors must be read out at the full LHC bunch crossing rate of 40 MHz. The current Hybrid Photon Detectors (HPDs), having an embedded readout electronics working at 1 MHz, will be replaced by Multi-Anode Photo-Multipliers Tubes (MaPMTs) equipped with a brand new external frontend electronics interfacing with the upgraded LHCb readout system [4]. The Photon Detector Module (PDM), comprising 16 MaPMTs, 128 CLARO ASICs and two digital boards, is the first level of modularity of the RICH upgrade detectors that can be interfaced with the new LHCb readout architecture.

2. – The RICH upgrade Experiment Control System

Following the strategy implemented for the current LHCb experiment [5], the ECS will handle the configuration, monitoring and operation of all the experimental equipment that will be installed in the upgraded LHCb detector. Each subdetector needs to develop its own ECS that will be integrated in the LHCb ECS during normal operations.

Fig. 1. – Example of some user interfaces used to operate the system through the RICH upgrade ECS prototype.

The control systems of the experiments at the LHC are developed using the WinCC-OA Supervisory Control and Data Acquisition system [6], with guidelines, conventions and tools provided by the Joint Controls Project (JCOP) [7], developed at CERN. The automation and sequential procedures required by the ECS are achieved through the Finite State Machine (FSM) concept making use of the SMI++ object oriented framework [8] and using the DIM protocol [9].

The prototype of the RICH upgrade ECS integrates in a FSM all the control systems required by the experimental setup to work, allowing automated and sequential procedures. The operations of the setup are done through user interfaces, as shown in fig. 1. The RICH_DCS sub-system includes the control and monitoring of the experimental equipments required by the detector to work, including low-voltage power supplies and temperature sensors. The RICH_HV sub-system comprises the control and monitoring of the high-voltage power supplies. The RICH_DAQ sub-system is responsible for the configuration, control and monitoring of the frontend and readout electronics. A run control and the tools to monitor the setup are also available.

The frontend electronics is configured, controlled and monitored using the prototype of the PCI express that will implement the upgraded LHCb readout architecture, namely the MiniDAQ. The LHCb Online group provides users with a generic FSM and with the tools required to setup the DAQ system for each subdetector [10]. On the other side, the specific functionality required by each subdetector must be implemented by the corresponding group. Regarding the RICH detectors, these functionalities include the automated procedures to calibrate the opto-electronics chain in order to maximize the photon detection efficiency. These procedures comprise threshold, test pulse and timing scans. Threshold scans allow to determine the integral of the pulse height spectrum of each MaPMT channel and are used to determine the CLARO threshold corresponding to the maximum signal-to-noise ratio. Test pulse scans allow to study the linearity (in terms of the correspondence between CLARO threshold and charge) and the noise of each CLARO channel. Timing scans allow to determine the latency of the DAQ system.

Automated actions related to the detector safety are implemented, *e.g.*, the switch-off of the high-voltage and low-voltage power supplies in case any temperature sensor is reading values above the user defined limits. Thanks to the scalability foreseen by the control system, these features can be easily extended to other monitoring sensors and used within the higher multiplicity of the final RICH detectors.

The progresses achieved in the integration of the RICH frontend with the new readout architecture allowed to install and operate a PDM within the current RICH 2 detector. The module is placed on the back of the HPDs plane, hence partially receiving Cherenkov light from LHC collisions. The PDM is synchronized with the LHCb clock and trigger and it is controlled and monitored by a control system based on the RICH upgrade ECS prototype.

3. – The RICH upgrade inventory, bookkeeping and connectivity database

The large number of hardware units foreseen by the upgraded RICH detectors motivated the development of an inventory, bookkeeping and connectivity database. Given the necessity to interface the database with the LHCb ECS and standard databases during operations, it has been developed using WinCC-OA and the JCOP framework. The database will contain the calibration data of each component, the connectivity of the hardware units in the various level of modularity of the detector and the working point in terms of the high voltage applied to the MaPMTs and the configuration parameters of the frontend electronics. The capability to store the working point will be an important feature in particular during the final commissioning of the detector.

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