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The πLUP project: Exploiting new techniques and neural networks in high-energy experiment data acquisition

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Summary. — The constant challenge to break the frontiers of energy and luminosity in high-energy physics experiments at LHC brings along the necessity of constant technological efforts in the acquisition of the signal generated by particles detectors. The relatively slow pace of the technological advance when compared to the constant increase of the outcoming bandwidth from the detectors requires the exploit of innovative methods and architectures for the data acquisition electronics. The πLUP project aims to create the prototype of a new generation of flexible data acquisition boards by exploiting the capabilities of the FPGA technology combined with the ease of use of an integrated Linux kernel, in order to implement new technological paradigms and to study the impact of neural networks in the reconstruction of acquired data.

1. – Motivations

The advancement of searches for new physics at the colliders, such as the LHC, requires an enormous read-out bandwidth to acquire data generated in the high-energy and high-luminosity *pp* collisions happening inside the accelerator at a frequency of 40 MHz. The read-out process is intrinsically highly parallelizable, making CPU-based solutions in general inefficient due to the sequential nature of their architectures, while the more efficient ASIC-based solutions are non-flexible and, therefore, impossible to fix or update over time. In the last few years, most of the data acquisition systems moved towards the direction of FPGAs, highly parallelizable devices ($\mathcal{O}(10^6)$ logic cells) whose functions are reconfigurable on the fly. The modern "brute-force" approach to data acquisition at large colliders is however starting to show limitations, as the future increase of luminosity (HL-LHC and beyond) will keep pushing the boundaries of the quantity of data to be read-out from the detectors each second and the data storage has to increase at least as fast as the read bandwidth. We need therefore a new approach for incoming data acquisition based on a flexible and a smart discriminant.

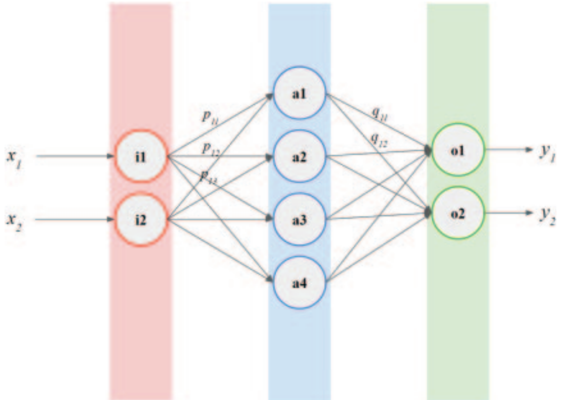

Fig. 1. – General structure of an artificial neural network with one input layer (red), one hidden layer (blue) and one output layer (green).

2. – Artificial neural networks

Artificial Neural Networks (NNs) are rising in popularity in applications of vastly different fields and provide a reliable way to automatically discriminate events of interest. In general, a NN is composed of three or more levels, called "layers", each containing artificial neurons. A vector of input signals x_i is transferred from the input layer to a hidden layer, as shown in fig. 1. Each signal x_i is bound to a weight p_{ij}; if $p_{ij} > 0$, the neuron a_j gets excited by the signal, otherwise the signal is inhibited. Each neuron a_j produces an output signal:

$$S_i = f\left(\sum_{i=1}^{n} p_{ij} x_i\right), \tag{1}$$

where $f(\,)$ is called activation function. The value of the weights p_{ij} can be set by training the NN using samples of input signals with well-known composition. More than 40 years passed between the introduction of the NNs and their use in high-energy physics. The spread of their use grows with the increase in complexity of the challenges and are currently used for real-time trigger systems, particle reconstruction in data analysis and signal simulation. A NN training sample for a signal of interest can be created by means of Monte Carlo simulations, allowing the coverage of a wide spectrum of physical cases.

3. – The πLUP project

While an approach for neural network implementation based on FPGA may be more complicate than a CPU- or a GPU-based one, the combination of intrinsic high parallelizability, flexibility of reconfiguration and optimization makes the FPGA solution a feasible way for both on-line and off-line operations. One of the main drawback of FPGA-based solutions is the toughness for the final user to program the board itself; in order to address this issue, the INFN Bologna group came up with the πLUP project.

The πLUP board (fig. 2) has been developed, built and tested by the INFN Bologna group [1] and aims to offer computational power, flexibility and ease of use. Its architec-

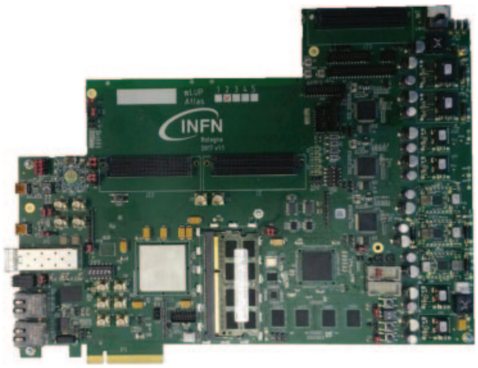

Fig. 2. – The πLUP data acquisition board.

ture is based on two FPGAs, working in a master/slave configuration: a Xilinx Zynq System-on-a-Chip (SoC), composed of an FPGA and an ARM CPU implemented on the same dice, acts as a master, while the computational efforts are left to a Xilinx Kintex FPGA. A high number of optical and electrical communication paradigms (PCIe, optical fibers, ...) offers flexibility in interfacing the board with a variety of systems [2]. Thanks to the CPU integrated in the Zynq SoC, the πLUP can easily operate fully fledged Linux distributions and execute `C` and `bash` code natively on the platform. The interface between the various components of the boards is based on the Xilinx AXI4 protocol, making it possible to add and operate new peripherals on the fly. The project is in an advanced state of development and a second revision of the board schematics is currently ongoing [3].

4. – Conclusions

The πLUP is a read-out board for high energy physics experiment, currently in development at INFN Bologna. The board is based on FPGA technology and aims to combine ease of use and parallelizability of the operations. Thanks to its flexibility, the πLUP is an ideal starting point to implement new paradigms in high-energy physics data acquisition and to become a common platform for different groups and experiments. The growing interest towards implementations of artificial neural networks is an important case study for the developement of future data acquisition systems.

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