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TIGER read-out for the new CGEM inner tracker off the BESIII experiment

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Summary. — TIGER (Torino Integrated GEM Electronics for Read-out) will be the innovative on detector electronics for the upgrade of the inner tracker in the BESIII experiment. The chip will allow the analogue read-out of the CGEM strips, making the merging of two different signal reconstruction algorithms possible improving the performance with respect to the main drift chamber (MDC) currently installed.

1. – CGEM-IT detector overview

The CGEM-IT (Cylindrical Gas Electron Multiplier Inner Tracker) is the detector proposed to replace the inner main drif chamber currently installed in the BESIII spectrometer. Indeed, the most inner layers of the MDC are losing gain due to the high luminosity of the experiment. Replacing this detector with 3 layers of triple GEM foils will improve the resolution along the beam direction, thus improving the secondary vertex reconstruction.

The signal, generated by the ionization in the drift region (fig. 1), is amplified and then collected on the anode strips. The analogue reading of the strips using TIGER ASICs will allow to implement the merging of μTPC (Micro Time Projection Chamber) and Charge Centroid reconstruction methods. A resolution of 130 μm [1] is thus obtained with a total of 10000 strips (25000 will be required by digital reading for the same performance).

2. – TIGER overview

TIGER is a mixed signal read-out chip [2] which implements the reading of 64 channels from the very front-end to the back-end, including bias generation, global and channel controls, an internal calibration pulse generator and the LVDS output.

In each TIGER channel, the signal is preamplified and then split into two different branches (fig. 2). One branch, with a faster shaper (rise time ∼60 ns), will be used for the signal time stamp. The other one, after a slower shaping (rise time ∼170 ns), will measure

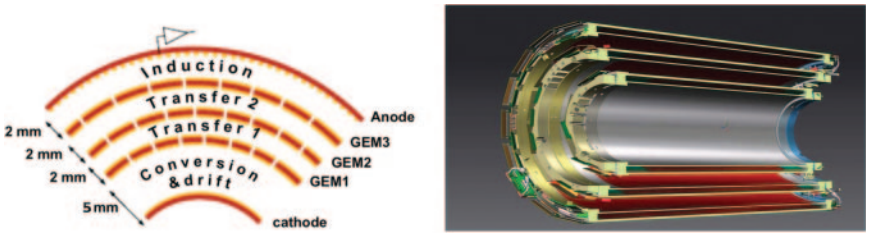

Fig. 1. – Single-layer internal layout (left) and full detector with 3 layers 3-D CAD (right).

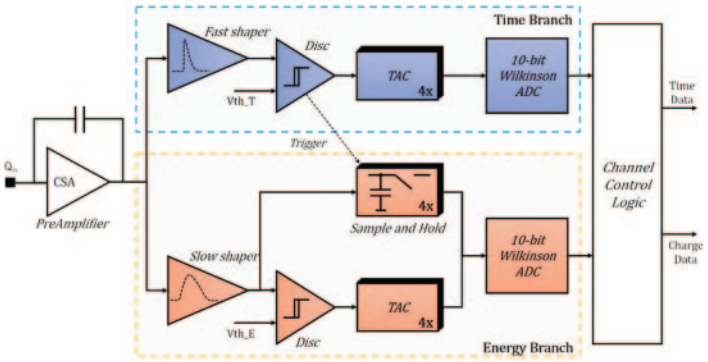

Fig. 2. – TIGER channel architecture.

the signal amplitude, allowing the use of Time Over Threshold or Sample and Hold techniques. The outputs of the two branches are then digitalized by Wilkinson ADCs, providing a 50 ps time binning at 160 MHz clock frequency, and the back-end electronics produces an amplitude and time signature in LVDS standard. TIGER can efficiently measure the amplitude of signals from 3 to 50 fC, with a maximum rate per channel around 1 kHz and a time resolution below 5 ns, meeting the detector specifications.

3. – TIGER test and optimization

The first version of TIGER (V0) was produced in 2016 and tested thoroughly in both back-end and front-end [3]. The final version of TIGER (V1), with an improved front-end, was produced in late 2017 and its test and optimization has taken place from January 2018. The ASIC is now ready for the final calibration and integration.

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