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ALPIDE for space applications: Power consumption

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Summary. — ALPIDE, a monolithic active pixel sensor developed for the ALIDE Inner Tracker upgrade, is studied as possible sensor unit for a space-borne particle tracker. The aspect of power consumption and heat dissipation is investigated.

Monolithic Active Pixel Sensors (MAPs) gained increasing importance in particle tracking. Already used in the STAR experiment at RHIC [1], they will be the base technology of ALICE Inner Tracker upgrade project at CERN [2]. MAPs in pixel amplification feature extremely low noise, very small pixel size (few tens of μm) and relatively low power consumption. This latter aspect is crucial for space applications, whose power budget is usually much lower than for ground experiments and where power dissipation is often performed conductively, bringing heat to the satellite cold plate.

1. – The case of HEPD

The reference case for this study is the High Energy Particle Detector (HEPD), a payload of the China Seismo Electromagnetic Satellite (CSES) designed and fabricated by the Limadou Collaboration. HEPD is sensitive to electrons and nuclei up to 200 MeV/n, with thresholds of 3 MeV and 30 MeV/n, respectively. To reconstruct the arrival direction of impinging particles, HEPD is equipped with two planes of double-sided microstrip detectors, each of them 300 μm thick and $210 \times 210\,\mathrm{mm}^2$ wide.

In view of a possible CSES-2 mission, we explore the possibility of replacing the tracker above mentioned with three planes of MAPs. This solution lowers the effective thickness of the tracker, lowering the experiment energy threshold. The event rate consequently increases, but pixel detectors do not present the problem of multi-hit degeneracy, as strip-based trackers do. To construct the tracker, we have chosen the ALPIDE sensor [2]. The tracker is organized in 5 independent modules, called turrets. Each turret is made of three overlaying staves, about $30 \times 150\,\mathrm{mm}^2$. MAPs are powered and controlled with a Flexible Printed Circuit (FPC). The same PCB is used to send out signals. The stave

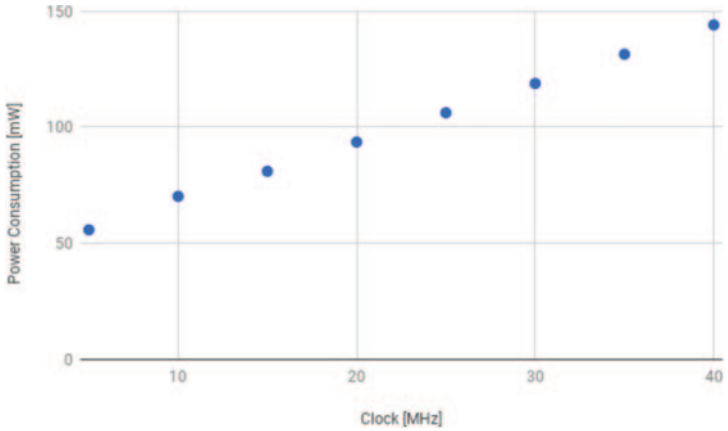

Fig. 1. – ALPIDE power consumption *vs.* CTRL line clock frequency.

is basically made of three layers: i) the FPC; ii) a group of 2×5 ALPIDE sensors; iii) a carbon fibre cold plate, in contact with sensors, ensuring mechanical stability and heat dissipation.

2. – Power consumption

The ALPIDE power need depends on the operation mode [2]. For the whole tracker described above the power consumption would be 24 W in inner barrel mode (12 W for the outer barrel mode), much higher than needed by the HEPD double-sided microstrip detector (about 4 W). We started a campaign of experimental tests to: i) independently measure the power consumption published by [2]; ii) measure starting and inrush currents; iii) implement solutions to decrease the need for power; iv) measure heat flows to conveniently parametrize the MAP in thermomechanical models. To this purpose, we used a single-chip laptop-driven setup, where ALPIDE is wire-bonded to a carrier board,

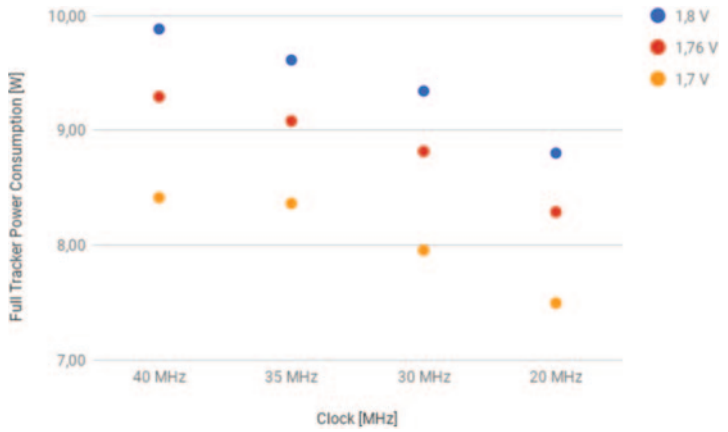

Fig. 2. – Five turrets power consumption during readout. Clock distributed to one turret per event.

connected to a MOSAIC readout board [3]. For both analog and digital front-ends (f.e.) the nominal power voltage is 1.8 V. Tests were performed down to 1.7 V (see fig. 2). We measured the current with a passive probe and an active probe. Since the power need of the analog f.e. is stable over time and independent of the operation mode, we focused our attention on the digital f.e.

Downclocking: Event rate and occupancy for the CSES-2 scenario are sufficiently low to avoid using the 1.2 Gbps serial line designed for the ALICE experiment. If ALPIDE is read out in space, it will happen through the slower control line (CTRL), usually clocked at 40 MHz. Using CTRL reduces the power consumption down to 120 mW/chip and allows to power off the PLL block, needing a 40 MHz clock. Routine tests have shown ALPIDE being responsive down to 5 MHz clock frequency, with power consumption decreasing linearly with the clock frequency (see fig. 1).

Clock gating: The HEPD-2 trigger could have the same modularity of tracker turrets, sufficiently close to each other to guarantee a 1-1 correspondence of trigger units and turrets. This solution allows to distribute the clock only to one turret per event and the total power consumption would be just 8 W for the full tracker in idle, with only 10 W during the event readout, as shown in fig. 2 (inner barrel mode).

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