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The ATLAS tracking system for HL-LHC

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Summary. — The current inner detector of the ATLAS experiment will be replaced with a new, all-silicon detector to cope with the tough environment of the High Luminosity LHC (HL-LHC). The instantaneous luminosity of HL-LHC would result in harder conditions for the detector: increase in occupancy, bandwidth and radiation damage. The Inner Tracker (ITk) will consist of an inner pixel and outer strip detector aiming to provide tracking coverage up to $|\eta| = 4$. The layout of the pixel detector is now finalized with five layers of pixel silicon sensor modules in the central region and several ring-shaped layers in the forward region. Due to their radiation hardness, 3D sensors are a promising option for the innermost pixel layer while in the other layers planar sensors will be used. The required very high hit-rate capabilities, increased pixel granularity, extreme radiation hardness and reduced material budget call for a size reduction as compared to existing sensors, involving smaller pitch, reduced active thickness and lower power consumption. All hybrid detector modules will be read out by a new front-end chip, developed within the RD53 Collaboration, connected to the silicon sensors using bump bonding. From simulations, the ITk performance in terms of tracking and vertexing is expected to be similar or better than that of the current tracking system, despite being in a much harsher environment.

1. – Introduction

The High Luminosity LHC (HL-LHC) aims to increase the LHC dataset by an order of magnitude in order to increase its potential for discoveries and precision measurements. The HL-LHC is expected to reach a peak instantaneous luminosity of 7.5×10^{34} cm^{-2} s^{-1}, yielding an average number of 200 proton-proton interactions per bunch-crossing (pile-up).

The granularity of the current Inner Detector (ID) [1,2] of the ATLAS experiment [3], composed of a silicon pixel, a silicon strip and a transition radiation detector, would not be sufficient to resolve the higher track density due to the larger pile-up, thus decreasing the physics potential in terms of precision of measurements and reach of searches.

Moreover, the track density would lead to the saturation of the bandwidth. Finally, the detector would not be able to work efficiently with the HL-LHC radiation doses.

To cope with the resultant increase in occupancy, bandwidth and radiation damage, the ID will be replaced by a new all-silicon system: the Inner Tracker (ITk). The ITk will be made by pixel and strips detector modules arranged in layers, reaching an angular coverage of $|\eta| = 4$, larger than the current ID ($|\eta| = 2.5$). This will help to provide a better reconstruction of forward leptons and to mitigate pile-up effects, especially in jet reconstruction.

2. – Detector layout

The layout for ITk was first presented in the Technical Design Reports [4,5]. The Pixel detector (now finalized [6]) has five layers of silicon pixel sensor modules in the central region and several ring-shaped layers in the forward region, while the strip detector includes silicon microstrip sensor modules arranged in four layers and and six rings per each quadrant (see fig. 1).

In particular, for the pixel detector, the modules are placed in parallel to the beam axis in the η low region, while in the high η region (endcaps) they are placed perpendicular to the beam axis. In the intermediate region, the modules will be tilted at an angle with respect to the beam axis (inclined section). The first two layers are expected to be replaced after $2000\,\mathrm{fb}^{-1}$, since the radiation damage accumulated in years of operation would affect the functionality of the modules, both the sensor and the chip components.

The ITk detector has an important reduction in the material budget (a maximum of 2 radiation lengths across the angular acceptance) with respect to the ID (up to 6 radiation lengths). New solutions are going to be deployed for the pixel modules to reach this purpose: *i.e.*, serial powering and inclined supports, maximising the resolution and minimizing the required material.

3. – Focus on pixel module

The pixel module is the result of the assembly of three main components: silicon sensor, read-out chip and flexible circuit. The chip is connected to the sensor using the bump bonding technique, with a bump bond density of 4×10^4 pixels per cm^2, an order of magnitude higher than the current detector pixel modules. Then the flexible circuit is glued on top of the sensor and connected to the read-out chip through aluminum wirebonds.

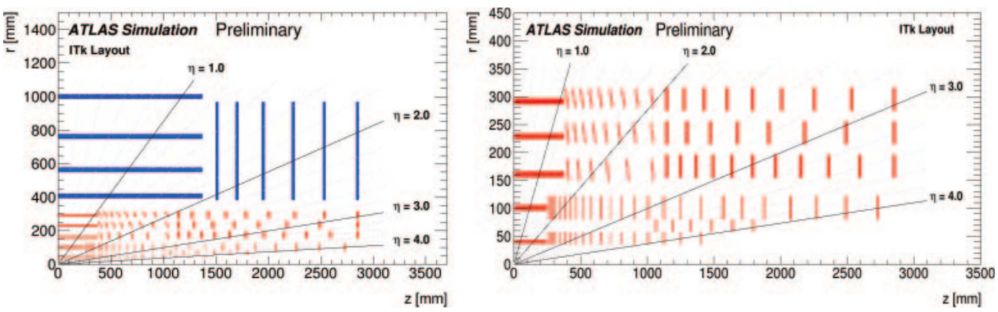

Fig. 1. – The inner tracker detector layout (left) and a focus on the pixel detector (right) [6].

The pixel detector will be made by a total of about ten thousands hybrid pixel modules, with planar sensors in the outermost layers and 3D sensors in the innermost layer (layer 0). The planar sensors will be 150 μm thick in the layers from 2 to 4 and and only 100 μm thick in the layer 1. The 3D sensors, with electrodes implanted vertically inside the silicon structure, will have a total active thickness of 150 μm, plus 100 μm of silicon for support. The benefit of having 3D sensors in layer 0 is their increased radiation resistance, thanks to the shorter drift length for the charge carriers and the much decreased depletion voltage, expecially after significant radiation dose. The pixel cell geometry, not yet determined, can be square ($50 \times 50\,\mu\text{m}^2$) or rectangular ($25 \times 100\,\mu\text{m}^2$).

The read-out chip with 65 nm CMOS front-end electronics is being developed within the RD53 Collaboration, in a joint effort between the ATLAS and CMS experiments. The first prototype, RD53A [7], hosts three different analog front-end designs, identified as differential, linear and synchronous, to allow the evaluation of different technologies in view of the final chip design. The ATLAS chip will consist of a pixel matrix of 400×384 pixels, being compatible with both pixel cell geometries.

4. – Tracking performance

Despite the increase in complexity of the project and the tougher conditions, the tracking and vertexing performance of the ITk detector are expected to be similar or better to the current tracking system. The simulations performed on $t\bar{t}$ events show that the ITk detector will maintain a good track reconstruction efficiency across the whole angular range with pile-up levels expected at the HL-LHC, compared to the Run 2 ID performance (see fig. 2). Similarly lower fake rates are expected, with the fake rate defined as the fraction of tracks not corresponding to a single simulated particle traversing the detector.

Despite the increase in pile-up density, the ITk detector is expected to have higher vertex reconstruction efficiency compared to the Run 2 ID performance (see fig. 3, left). The quality of the vertexing performance is almost constant within the range of expected pile-up density, thanks to its extended angular acceptance and high granularity. Similarly, the resolution on the z coordinate of the primary vertex will be significantly improved,

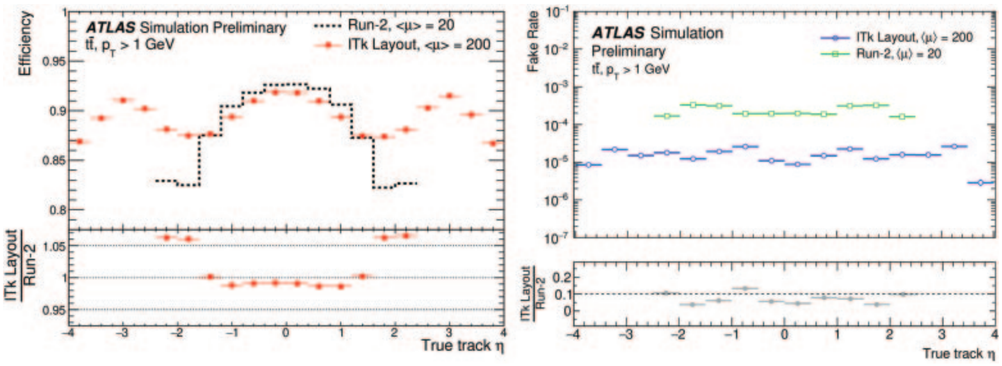

Fig. 2. – Track reconstruction efficiency (left) and fake rate (right) expected for the ITk detector at the pile-up level of HL-LHC, compared to the performance of the ID at the Run 2 pile-up level [6].

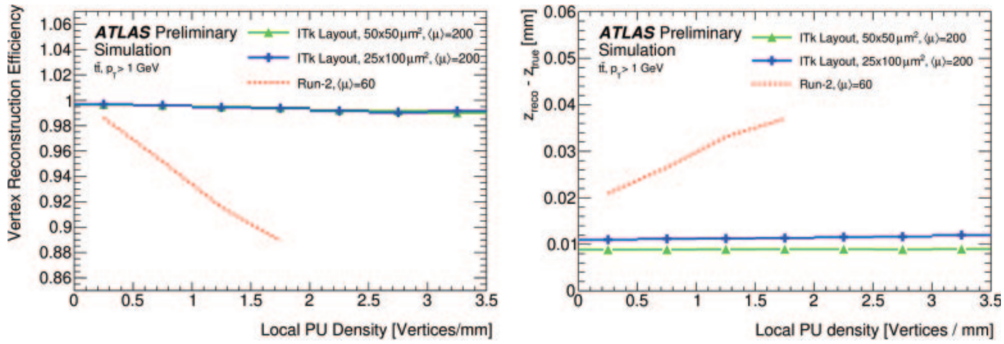

Fig. 3. – Vertex reconstruction efficiency (left) and primary vertex z coordinate resolution (right) expected for the ITk detector at the pile-up level of HL-LHC, compared to the performance of the ID at the Run 2 pile-up level. The effect of having square or rectangular pixel cells is shown as well [6].

ensuring high-quality tracking performance in a high pile-up environment (see fig. 3, right). The square pixel geometry would ensure a better z coordinate resolution with respect to the rectangular one. On the contrary, the longitudinal impact parameter of the tracks, d_0, would benefit from the rectangular pixel geometry.

The tracking and vertexing capabilities of the ITk detector will guarantee a similar or improved pile-up rejection (see fig. 4, left) and b-tagging performance (see fig. 4, right) with respect to the performance of the ID. In particular, the pile-up jet rejection is expected to be slightly better in the case of the square pixel cells compared to the rectangular one. Regarding the b-tagging performance, the rectangular pixel geometry, thanks to a better d_0 resolution, shows a significant improvement (10–20%) in light-jet rejection as a function of b-jet identification efficiency. Despite the larger inner radius, ITk can improve the b-tagging performance of the ID and, additionally, allows the possibility for forward b-tagging.

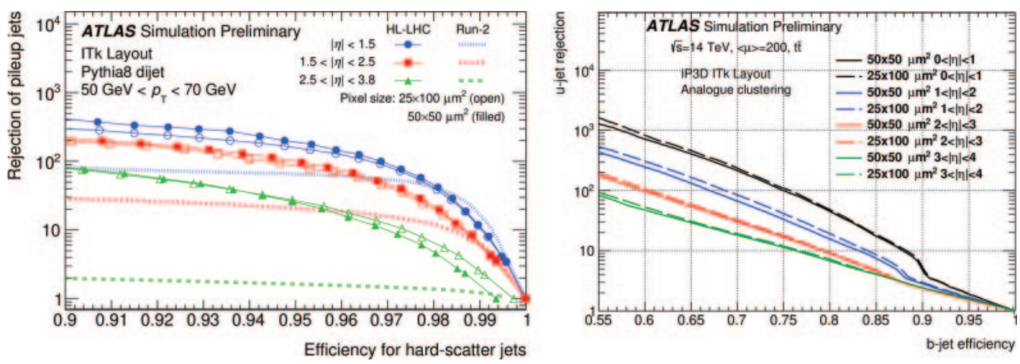

Fig. 4. – Pile-up jets rejection as a function of jet reconstruction efficiency (left) and light-jet rejection as a function of b-jet identification efficiency (right) expected for the ITk detector at the pile-up level of HL-LHC, compared to the performance of the ID at the Run 2 pile-up level. The effect of having square or rectangular pixel cells is shown as well [6].

5. – Conclusion

In view of the HL-LHC phase, the current ID will be completely replaced by the ITk detector. Compared to the Run 2 ID performance, ITk is expected to reach a similar or even better tracking and vertexing performance despite the more challenging run conditions. In particular, the extended angular acceptance (from the ID acceptance of $|\eta| < 2.5$ to the ITk $|\eta| < 4$) will guarantee a better reconstruction of forward leptons and mitigate the pile-up effects.

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