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Results of multi-module system test for the ATLAS ITk Endcap detector(*)

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Summary. — With the beginning of the High Luminosity phase of the Large Hadron Collider (LHC) in 2027, the ATLAS detector will have to cope with harsher radiation levels and increased pile-up. To face these challenging conditions the ATLAS inner detector will be completely replaced with a new all-silicon tracking system: the Inner Tracker (ITk). ITk will consist of a pixel detector at a smaller radius and a large area strip detector surrounding it. The pixel detector is equipped with hybrid detectors read out by novel ASICs implemented in 65nm CMOS technology. To save material in the servicing cables, serial powering is employed for the supply voltage of the readout ASICs. This paper will give an overview of the first prototype multi-module system test realized for the ITk outer endcaps focusing on the serial powering scheme implemented via the pre-production on-detector electrical services.

1. – Introduction

The High Luminosity [1] era of the LHC [2] will bring the instantaneous luminosity of the machine up to $7.5\cdot 10^{34}$ cm^{-2} s^{-1} and the maximum number of proton-proton collisions per bunch-crossing close to 200. The integrated luminosity of about 350 fb^{-1} expected at the end of Run 3 is foreseen to reach 4000 fb^{-1} after 10 years of operation in high luminosity conditions. The increased number of collisions will set more challenging requirements in terms of radiation hardness, read-out electronics and triggers for the experiments. The current tracking system of the ATLAS [3] detector is not suitable for the high luminosity scenario. The Inner Tracker (ITk) [4], based on pixel and silicon strip detector technologies, will be the new all-silicon tracker completely replacing the current Inner Detector (ID). After the approval of the TDRs by the CERN Research Board, the pre-production readiness phase has started at the institutes involved and the community is now moving into production mode.

2. – ATLAS ITk pixel endcaps overview

The current ATLAS ID, consisting of silicon pixel, silicon strip detectors and transition radiation tracker is going to be replaced with the ITk: the new all-silicon tracker. The

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TABLE I. – *Layout of one endcap of the ATLAS ITk pixel detector* [4].

Layer	Radius [mm]	Rings	Modules per Ring	Total number of modules
Layer 2	174.60	11	32	352
Layer 3	234.65	8	44	352
Layer 4	294.70	9	52	468

ITk will consist of 13 m^2 of pixel detectors with 5 billion read-out channels and 160 m^2 of strip detectors with 50 million read-out channels [4, 5]. The 5-layer layout of the pixel detector provides extended coverage up to $|\eta| < 4$ minimising multiple scattering effects by greatly reducing the material budget compared to the current ID. The pixel detector is organised into three mechanically independent sub-systems. An Inner System (IS) includes the first two innermost pixel layers (Layer 0, 1) and an Outer System (Layer 2, 3, 4) that includes an Outer Barrel (OB) with the three outermost pixel layers of flat staves and inclined sections, and two Outer Endcaps (ECs), built by three pairs of concentric carbon fiber half-shells per side hosting Half-Ring (HR) shaped carbon fiber supports populated with modules.

The construction of one endcap each has been procured by Italy and the UK. In Italy, the INFN laboratories of Genova, Lecce, Milano and Frascati are involved in the construction and integration of the Italian EC. In the ECs modules are glued on a carbon half-ring structure using a precision pick&place machine, during the so-called loading procedure. The number of modules loaded on each HR varies depending on the layer and it is summarized in table I. The ITk cooling system is CO_2 based and the HR are cooled through a titanium pipe which is placed inside the HR. The pixel modules in the outer systems are arranged in quad-modules and consist of four FE chip tiles flip-chipped to a single planar sensor tile of 4x4 cm^2 area; both FE chips and sensor have pixel pitch 50x50 μm^2. Readout chips on a pixel quad-module are powered in parallel using up to 9.46 W of power. By powering up to 14 of those modules in series in a chain, the amount of required cables is reduced and thus the material budget in the detector. This is made possible through the shunt-LDO (SLDO) powering mode of the FE chip by providing the chip with a constant and redundant power budget [6]. The serial power scheme is implemented through the on-detector services that consist of a flexible PCB circuit called bus tape which is loaded on the HR, modules are connected to the bus tape via a flexible PCB (*power pigtail*) welded on the bus tape and plugged into the module with a mechanical connector. Moreover, the bus tape hosts a monitoring chip (MOPS) that is used to monitor modules temperature and voltage drops.

3. – Prototypes realized in the Italian laboratories

A first pre-production layer 4 HR loaded with modules and on-detector services has been realized in the spring of 2023 to demonstrate the feasibility of loading and testing procedures before moving to the production phase. The mechanical carbon fiber structure of the HR has been realized in the Genova site during winter 2023. The HR met all the thermo-mechanical specifications requested in the ITk project. In March 2023 two pre-production quad modules were loaded on the HR after several stand-alone tests to validate their electrical performances. The module loading procedure validated the performances of the pick&place method, showing that the machine is able to place the modules in their nominal position with respect to the HR within the requested tolerances for an hermetic particle tracking. A critical aspect of this process is the control of the SE4445 adhesive thickness between the module and the HR, which must ensure good thermal conductivity between the two parts and ensure module flatness in relation to the HR. The thickness of the glue was then measured after the loading using an optical profilometer showing that the pick&place method can guarantee a thickness between 50 μm and 200 μm, in agreement with the ITk thermo-mechanical specification. A pre-production bus tape was glued on the same HR using custom tools that guaranteed precision placement of the bus tape with respect to the modules within an error of 200 μm which is the tolerance required to allow the soldering of the power pigtail on the bus tape. The soldering of the power pigtail was done using a custom machine designed and produced in Genova that can control and monitor the force applied on the HR and the temperature of the soldering head during the welding process.

4. – Multi-module system tests results

After the realization of the layer 4 HR described in the previous section, the object was tested following the Quality Control (QC) and Quality Assurance (QA) procedures provided for the project. The QC/QA procedure of the modules consists of the validation of the electrical properties of the FE chip, the physics performance of the planar sensor and the validation of the connection of the two parts via the bump-bonding procedure. Several communication tests with the FE electronics are performed using a set of built-in injection circuits in the chips to prove the working of both the digital and analog read-out of them. Particular attention shall be paid to the FE chips threshold tuning and to the electronics noise, which is a good indication of the bumps quality: the connection of the FE pixel to its sensor pixel increases the capacitance of the read-out circuit and thus the noise so that pixels with lower electronics noise will be the disconnected ones. The performance of the sensor are checked using an X-ray source.

The module read-out is based on a full electrical chain read out by an FPGA card equipped with a dedicated firmware and software [7] (An optoelectrical read-out chain will be implemented for the pre-production phase). Modules loaded on the HR have been tested for the very first time in the serial powering scheme using the bus tape. The loaded HR has been thermally cycled with 10 cycles between -55°C and +60°C to prove the quality of the hybridization and the strength of all mechanical interfaces. Threshold and noise results of one of the two modules in the serial powering scheme before and after the thermal cycles (TCs) are reported in fig. 1 as a function of the PixelID defined as follows: PixelID = $384 \cdot \text{pixel}_{column}$ / pixel_{row}. Results do not show any significant change after the loading procedure. The HR was also used as the first test bench for the MARTA (*Monoblock Approach for a Refrigeration Technical Application*) [8] CO_2 chiller in the Lecce site. The MARTA system is based on CO_2 and it can reach a cooling power of 300W at -30°C. To date, we are able to cool the modules by circulating bi-phase CO_2 evaporation inside the HR titanium pipe. The temperature of the two modules has been monitored via the bus tape and the MOPS chip using a custom WinCC/ESP-32 based system, proving the functionality of the MOPS loaded on the bus tape.

5. – Conclusions

The ATLAS ITk pixel detector endcaps will be made of three layers of concentric carbon fiber half-shells per side hosting HR populated with quad modules. A pre-production

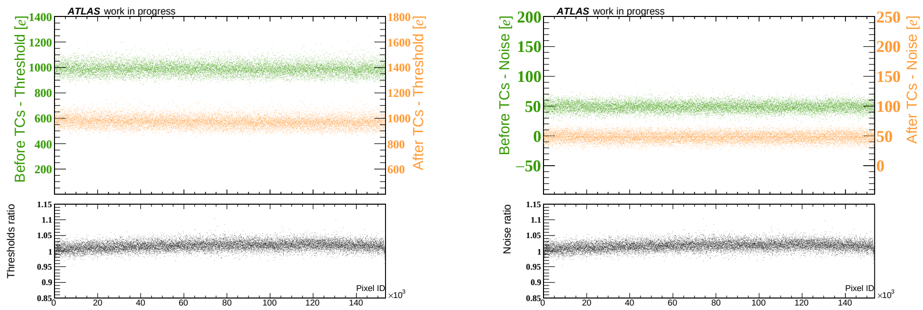

Fig. 1. – Threshold (left) and noise (right) of a pixel module are plotted before and after thermal cycles as a function of the pixel ID. The ratio of both, before and after thermal cycles, is plotted at the bottom of the figures, no significant changes have been observed.

layer 4 HR was realized in the spring of 2023 matching all the mechanical specifications of the project. The HR has been loaded with two pre-production modules and the on-detector services validating the pick&place machine. Modules, loaded on the HR, have been tested for the very first time in the serial powering scheme via the bus tape and power pigtails connectors, showing performances closer to the stand-alone test. The populated HR has been thermally cycled validating the strength of all mechanical interfaces and the modules hybridization quality. A first test of the MARTA cooling system was also successfully carried out, and the temperatures of the modules have been monitored for the first time using a MOPS chip loaded on the bus tape.

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