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The ALICE ITS3 upgrade project: Latest results on monolithic pixel sensors test structures realized in a 65 nm technology(*)

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Summary. — ALICE (A Large Ion Collider Experiment) at CERN investigates the properties of the quark-gluon plasma formed in heavy ion collisions at high energies. A crucial aspect of this research is the precise reconstruction of low momentum particles (< 1 GeV/c). The ALICE Inner Tracking System (ITS) plays a central role in this effort, it is the first large-area silicon tracker constructed entirely from Monolithic Active Pixel Sensors (MAPS). The ITS upgrade project will lead to a new detector, named ITS3, which will be equipped with three layers of sensors based on the latest 65 nm CMOS imaging process, developed by TPSCo foundry, enabling wafer-scale sensor production through advanced stitching techniques. This paper discusses the recent progress in the ITS3 project, highlighting the performance of thinned and bent sensors, the assembly process, and air cooling system. Initial test beam results match the small test structure desired characteristics, ensuring efficient detection and high spatial resolution. The first stage of project will be completed with the ITS3 installation, which is expected in LHC Long Shtudown 3 (2026-28). Commissioning and operation will follow.

1. – Introduction

ALICE (A Large Ion Collider Experiment) at CERN is designed to explore the properties of the quark-gluon plasma produced in heavy-ion collisions at high energies [1].

A key feature offered by the ALICE apparatus is the precise reconstruction of low momentum particles, less than 1 GeV/c. Accurate tracking of such particles, with an impact parameter resolution lower than 10 µm [2], is essential for probing the dense, high-temperature environment of quark-gluon plasma and requires highly advanced detector technologies.

Central to this effort is the ALICE Inner Tracking System (ITS), which is the first large-area silicon tracker constructed entirely from Monolithic Active Pixel Sensors (MAPS) [2]. These sensors offer superior spatial resolution (as low as 5 µm), with respect to ITS1, and low material budget (around 0.3 % x/X_0 per layer for the inner layers), which are crucial for minimizing multiple scattering.

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The ITS2 is currently employing the ALICE Pixel Detector (ALPIDE), a highly specialized chip developed specifically for this application [3]. The ALPIDE chip, made by Tower Jazz in the 180 nm CMOS imaging process, features innovative designs that enhance signal processing, ensuring a fast readout speed of up to 100 kHz, and detection efficiency higher than 99%, enabling the precise tracking of particle trajectories even in the high-multiplicity environment typical of heavy-ion collisions.

A replacement of the three innermost vertexing layers of ITS2 is foreseen during LHC long shutdown in 2026-28. The ITS3 will be the first truly cylindrical wafer-scale MAPS mounted in a vertex detector [4, 5]. The innermost layer will be closer to the interaction point thanks to a new, smaller beam pipe, having a radius of 16 mm and a thickness of only 500 µm. The main requirements of the ITS3 sensor ASIC are reported in table I.

The technology selected for the chip realization is the TPSCo (Tower Partner Semiconductor Company) 65nm CMOS imaging process. It guarantees a higher circuit density, the possibility to use the stitching technique over 300 mm wafers. Thanks to the stitching, selected parts of the reticle, called repeated sensor units (RSU), can be placed next to each other on the wafer during production to form a wafer-scale sensor.

The wafer-scale chips are, then, thinned to 50 µm in order to gain the required flexibility to be bent in the semi-cylindrical shape to the target radii: 19 mm, 25.2 mm, and 31.5 mm for layer 0,1, and 2 respectively.

The mechanical support is made with carbon foam ribs with low density and high thermal conductivity in order not to contribute to the overall material budget of the detector, see fig. 1.

The main benefits of such a device are: the extremely low material budget, 0.07% radiation length, and a homogeneous material distribution.

The present paper shows the results on the 65nm CMOS technology qualification campaign and the performance of the thinned and bent sensor. The ITS3 assembly is presented as well as the compliance with the experiment scientific constrains. As a final result, the performance of the stitched wafer scale sensor will be shown.

2. – Technology validation and bending

2˙1. *65 nm CMOS technology qualification campaign.* – The first investigation of the TPSCo 65 nm CMOS technology was conducted through the Multi Layer Reticle 1 (MLR1) submission. Several test structures were produced featuring different sensors doping levels and pixel matrix with pitches ranging from 10 to 25 µm were investigated.

TABLE I. – *ASIC main requirements*

Single point resolution	$\leq 5\,\mu m$
Pixel pitch	$< 25\,\mu m$
Fill factor (fractional sensitive area)	$> 92\%$
Detection efficiency	$> 99\%$
Fake-hit rate	< 0.1 pixel^{-1} s^{-1}
Fake-hit occupancy (10 µm Frame Duration)	$< 10^{-6}$ pixel^{-1} frame^{-1}
Fraction of Pb-Pb interactions fully recorded, Layer 0	$> 99.9\%$
Power Dissipation Density, Active Region	$< 40\,mW cm^{-2}$
NIEL	10^{13} 1 MeV neutron equivalent cm^{-2}
TID	10 kGy
Target Operating Temperature	15 °C to 30 °C

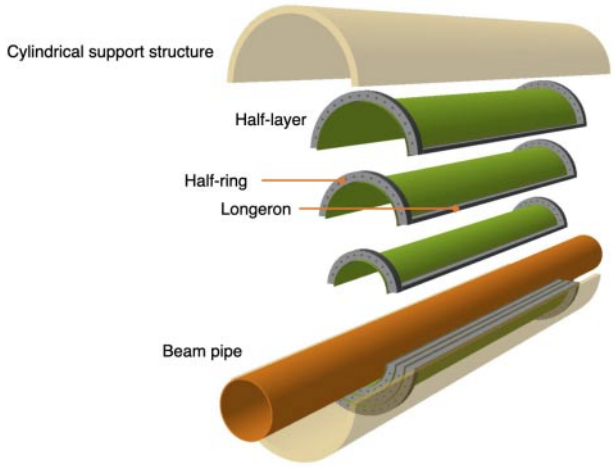

Fig. 1. – Sketch of ITS3 Detector layout. The 3 top and 3 bottom half layers are drawn around the beam pipe within the cylindrical support structure supported by carbon fibre foam half-rings and longerons [5].

Concerning the chip response characterization, the analogue and digital in pixel circuits were studied separately through three different test structures:

- an analogue pixel test structure (APTS) to test the analogue response of the sensor. It features a 4×4 pixel matrix with 10, 15, 20 and 25 µm pitches and a direct analogue readout;
- a digital pixel test structure (DPTS), equipped with a digital front-end chain, hosting a discriminator and a digitaser in-pixel, allows qualification of the pixel cell and the front-end chain (including the discriminator) as prototype for the final ITS3 sensor ASIC. It has a 32×32 pixel matrix with a 15 µm pitch and a digital asynchronous readout;
- a circuit exploratoire (CE65), featuring a large pixel matrix equipped with a rolling shutter analogue readout, for studying the uniformity of the detector response from a large matrix. This was realized in two versions: a 64×32 matrix and a 48×32 with 15 µm and 25 µm pixel pitches respectively.

The sensor performance was improved optimizing the implantation process. The study is based on the work done in the 180 nm TowerJazz imaging technology, and further optimized in the 65 nm TPSCo technology [6].

Three sensor process variants were developed (c.f. fig. 2):

- the standard process, similar to the one used in ALPIDE [3], features a collection electrode grown on a p-type substrate with low resistivity;
- the modified process, with a low dose n-type implant located below the collection diode and covering the whole pixel area;
- the modified with gap process, similar to the modified with the addition of lateral gaps to reduce the charge sharing among pixels.

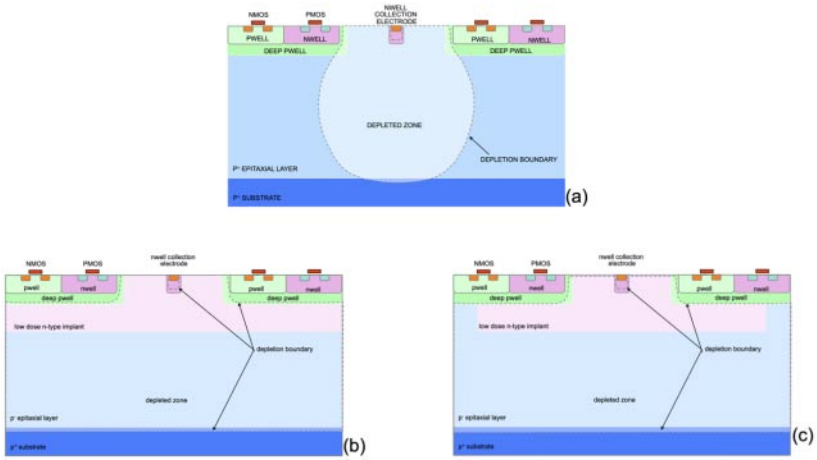

Fig. 2. – Sketch of the cross section of three pixel process designs: standard (a), modified (b), and modified with gap (c) [5].

The MLR1 submission demonstrated several key findings [7, 8]. First, it showed that the process modifications with gap reduces the cluster size regardless of the pixel pitch. Additionally, the detector can operate without applying a reverse bias, and radiation up to 1×10^{13} 1 MeV neutron equivalent fluence has a negligible effect on charge collection efficiency and resolution. The detection efficiency is maintained for pixel pitches up to 25 µm, and a spatial resolution better than 5 µm can be achieved with pixels smaller than 22.5 µm. Furthermore, the in-pixel front end implementation achieves a fake-hit rate below 0.01 pixel^{-1} s^{-1} while maintaining the required detection performance.

2˙2. *Bent chip performance*. – The APTS and ALPIDE bent sensors were characterized to evaluate their performance post-bending. The tests aimed to assess the number of non-responsive pixels, the threshold for each pixel, the noise levels, and the fake hit rate. Results obtained from ALPIDE chips bent along different axes and to various radii (cf. fig. 3) indicate that bending does not significantly affect the performance of the chip

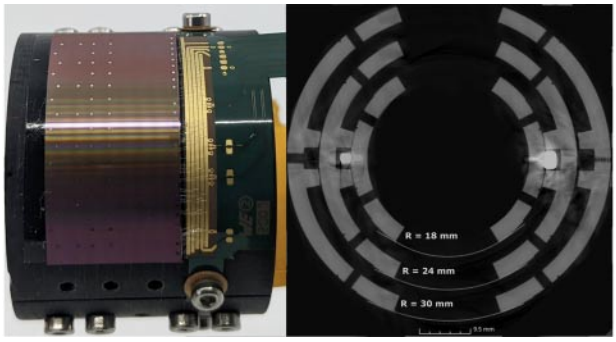

Fig. 3. – On the left, a photograph of the ALPIDE chip bent to a radius of 18 mm fixed onto cylindrical jig. On the right, a computer tomographic scan of three cylindrical jigs with attached the ALPIDE chips at the nominal radii foreseen for ITS3 detector [5].

keeping, for the normal operation value of the threshold around $100\,e^-$, the inefficiency below 10^{-4}.

Furthermore, the ^{55}Fe spectra collected at a reverse bias voltage of 4.8 V with bent APTS samples were compared to the spectra measured with a planar APTS. The analysis confirms that bending does not significantly impact the performance of the 65 nm technology-based APTS test structures [5].

3. – ITS3 assembly and cooling

The ITS3 tracking detector is split into two halves which are separately mounted around the beam pipe (cf. fig. 1). The half-layers are, then, bonded together to achieve an ultralight and stable assembly. In order to provide a mechanical support to the detector, the outermost layer is attached to an external cylindrical structural shell.

Prototypes based on the engineering model 1, shown in fig. 4, were employed to validate the integration principle including the air cooling approach.

The carbon foam serves as a spacer at the edges of the sensor, provides cooling, acting as radiator, while carbon longerons, glued along the chip borders, ensure rigidity with a minimal contribution at the material budget.

Another strategy followed to keep the material budget as low as possible, is the use of air flux for cooling. An air speed of 8 m/s guarantees a power dissipation of $40\,mW/cm^2$ with a maximum temperature gradient of 5 °C, as shown in fig. 5(a).

According to the aeroelastic tests (cf. fig. 5(b)), the displacement caused by the air flux at nominal speed is five times smaller than the target spatial resolution of the chip, therefore we do not expect major effects on the tracking.

4. – Stitched wafer-scale sensors

A large Monolithic Stitched Sensor (MOSS), about 259 mm × 14 mm, was designed and submitted in the first engineering run (ER1) to define the layout and stitching parameters for the subsequent full scale wafer sensor.

The MOSS, shown in fig. 6, features ten Repeated Sensor Units (RSUs) made with the stitching technique and accounting for 6.72 million pixels. They are terminated on the two extremities by two smaller end cap regions. The RSU is then subdivided in two half-units with pixel arrays of different pitches, 22.5 µm and 18 µm respectively. The two

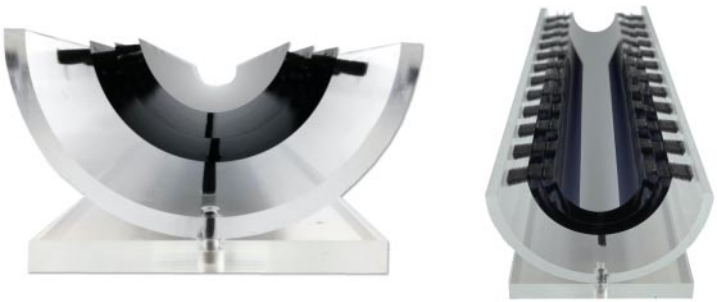

Fig. 4. – Engineering Model 1. Front and perspective of the engineering model 1 composed by three wafer-size blank silicon pieces, simulating the half-layers, stacked with carbon foam wedges at the silicon edges.

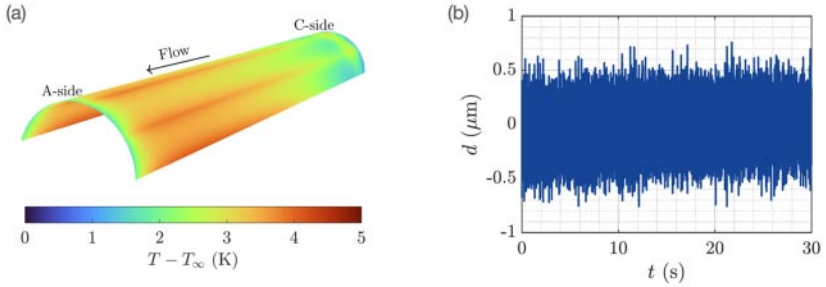

Fig. 5. – (a) Simulation of the half-layer 1 temperature gradient for an air speed of 8 m/s. The reference temperature used to evaluate the heat transfer coefficient is inlet air temperature (T_∞). (b) Aeroelastic measure of displacement at half-layer 2 center [5].

half units are characterised by different circuit densities, different widths and spacing of the interconnecting metal structures. Each half unit is a fully standalone functional unit with independent periphery, I/Os and powering in order to isolate small sensor regions in case of defects.

Regarding its performance, testing three wafers provided an initial evaluation of the powering fault density, which guided the design of the final sensor to meet the required yield. As regard the power yield, a maximum failure of 2% of the sensitive area is accepted. Based on these constrains, 67% of the tested sensors are suitable to be mounted in the ITS3. From the point of view of the powering yield, 18 wafers are needed to complete the full detector [5].

Regarding the next steps, initial results from test beam confirm the findings from the small test structure characterizations in terms of detection efficiency and spatial resolution. During ER2, a full-size, fully-functional prototype will be produced, followed by the final detector-grade production version in ER3. The optimization of detector integration and assembly will be evaluated through the production of two qualification models (two half-barrels). The final model will complete the detector with the production of additional four half-barrels.

5. – Conclusions

The innermost 3 layers of ALICE inner tracking system will be replaced with the first truly cylindrical wafer scale monolithic sensor. The first testing campaign allowed to validate the 65nm CMOS technology with the Multi Layer Reticle 1 submission, successfully demonstrated the possibility to implement the stitching technique to realize

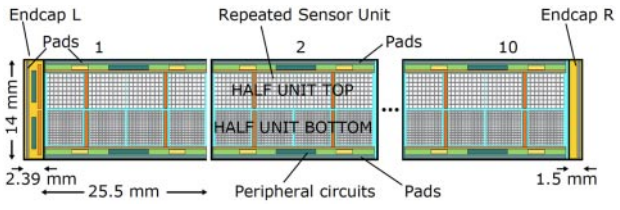

Fig. 6. – Draw of the MOSS chip with detail on its constituting parts [5].

a single 26 cm long sensor with the Engineering Run 1, and led to the production of the technical design report. Two more engineering runs are foreseen to prove the capability to integrate a wafer-scale bent sensor into the mechanical support, granting for heat dissipation through air cooling. The set in place of the detector is expected to start in 2026.

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