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System test for the Barrel Pixel Detector for the CMS HL-LHC Upgrades(*)

G. Bardelli(1)(2) on behalf of the CMS Tracker Group

(1) *Dipartimento di Fisica, Università degli studi di Firenze - Firenze, Italy*
(2) *INFN, Sezione di Firenze - Firenze, Italy*

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Summary. — The CMS Experiment will be upgraded in order to cope with the High Luminosity Phase of LHC (HL-LHC). The inner tracker will be completely replaced with a new detector capable of operating in the foreseen high level of radiation during HL-LHC. In order to power the pixel detector, while decreasing the passive material and limiting the radiation damage, a new scheme, based on serial powering, will be deployed, with a read-out system designed to work at high data rates. In order to verify that the components behave as expected when combined together, system tests are performed. The latest updates on the system test of the barrel Pixel Detector, having a full-scale system bench will be discussed in terms of threshold and noise. The latest results obtained with the optical read-out is also presented.

1. – The upgraded CMS inner tracker for the High Luminosity Phase at LHC (HL-LHC)

The High Luminosity Phase of LHC will push the luminosity towards unprecedented levels, delivering a maximum instantaneous luminosity of 7.5×10^{34} cm^{-2}s^{-1} and aiming to collect up to 4000 fb^{-1} of integrated luminosity from 2029.

The current CMS [1] tracker won't be capable to sustain such dense environment and it will be completely replaced with a new detector. The Inner Tracker [2], IT, *i.e.*, the innermost tracker system based on silicon pixel detectors, will feature thin pixel sensors with 25×100 μm^2 cell to overcome the challenges posed by HL-LHC. The sensors are prototyped to withstand high level of fluences and to reduce the total occupancy thanks to the small pitch size. The sensors are bump-bonded and flip-chipped to the CMS Read-Out-Chip, CROC [3], a chip designed by a joint CMS and ATLAS Collaboration, RD53, and based on 65 nm CMOS technology. The flip-chips are wire-bonded to a passive interconnection circuit, the HDI, to form the modules, the smallest assembly that will equip the IT. Two module types are chosen to populate the IT, the quad with four ROCs connected to one sensor and the double with two ROCs connected to one sensor.

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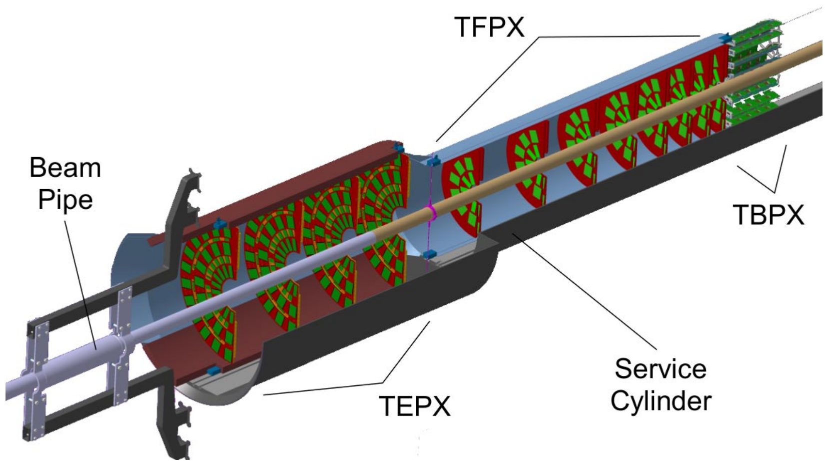

Fig. 1. – A schematic view of a quarter of the future inner tracker for HL-LHC, with the three subsystems highlighted.

The modules will be powered with an innovative power scheme based on serial powering [4] in order to deliver the required 50 kW for the full inner tracker while reducing the total amount of passive material. Other solutions, such as DC-DC converters, were discarded due to high level of radiation foreseen during HL-LHC. In order to guarantee the right powering to the ROCs of each module, a current shunt and a Low-Dropout regulator are combined into the ShuntLDO. The cumulative action of the two is to present the serial chain as a constant load to the power supply, while maintaining a even sharing of current between multiple chips powered in parallel in the same module.

A sketch of a quarter of the future inner tracker is shown in fig. 1. In the figure the subsystems are highlighted: TBPX for the Barrel, TEPX for the Endcap and TFPX for the forward disks that will increase the tracker acceptance up to $|\eta| = 4$. This paper will focus on the realization and the measurement of a system test emulating TBPX with the full-scale prototype of the read-out chips. The TBPX structure consists of 4 layers, each composed by ladders.

2. – TBPX system test with electrical flat cable read-out

The system test is realized using 8 TBPX quad modules. The module sketch and its components are shown in fig. 2, where also the cooling plate for the modules is shown. This is a layer in aluminium nitride that helps cooling the modules. These modules were wire-bonded at ETH Zurich and mounted directly on the mechanical structure at CERN. The modules are screwed directly to the prototype ladder and they are powered using a serial chain of 8 modules. The mechanical structure is close to final with the cooling pipes embedded inside the carbon fiber and carbon foam ladder. A bi-phase cooling based on CO_2 is employed. Four modules already mounted on the half ladder can be seen in fig. 2 on the left.

The modules available for this system test are bare modules, *i.e.*, there is no sensor flip-chipped to the CROC, only the HDI wire-bonded to the ROCs and the cooling plate. This system test was specifically designed to investigate the electrical properties of a serial chain of 8 quad modules, while the thermal measurements are not reliable for the

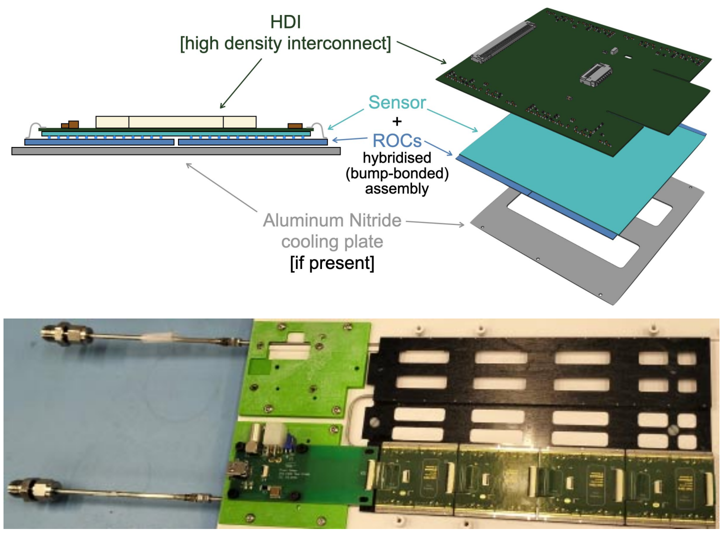

Fig. 2. – On the top a schematic view of a quad module and its components. On the bottom there is half ladder already mounted on the mechanical structure.

lack of sensors and the thermal paste between the modules and the ladder prototype.

In this preliminary implementation the read-out is performed through a flat cable of 15 cm that connects the modules to a custom adapter board that has a mini-dpi output to reach the DTC (Data Trigger and Control) implemented using a FPGA. The coolant mixture is controlled with a CO_2 pump with a temperature ranging from 20°C to -35°C. The system test is placed inside a cold box that can be set to -10°C where also dry air is flushed inside. The humidity and the temperature are monitored to prevent condensation.

The modules were powered with 8 Ampere requiring 14.4 V at the power supply. The powering of each half chain, *i.e.*, a serial chain of four modules only belonging to the same half ladder, is consistent between the two and considering the 8 modules powered together. The CO_2 temperature has been varied between 10°C and -31°C, without any significant difference in the module response or consumption. The modules have been calibrated at -31°C and the results in terms of threshold, noise and number of masked pixels were compared with standalone measurements of the modules at room temperature

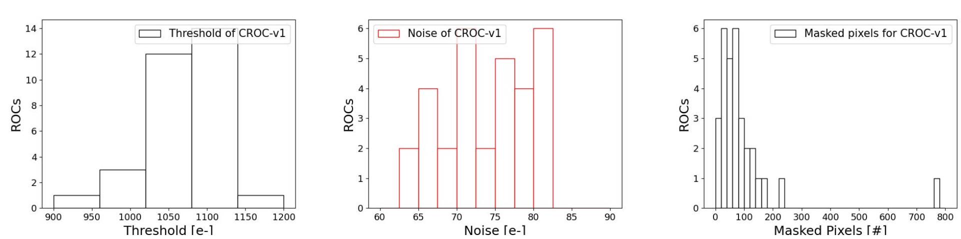

Fig. 3. – The results of the calibrations for the 8 modules powered in series. Left are the thresholds, center is the noise of the tuned ROC and right there is the number of masked pixels.

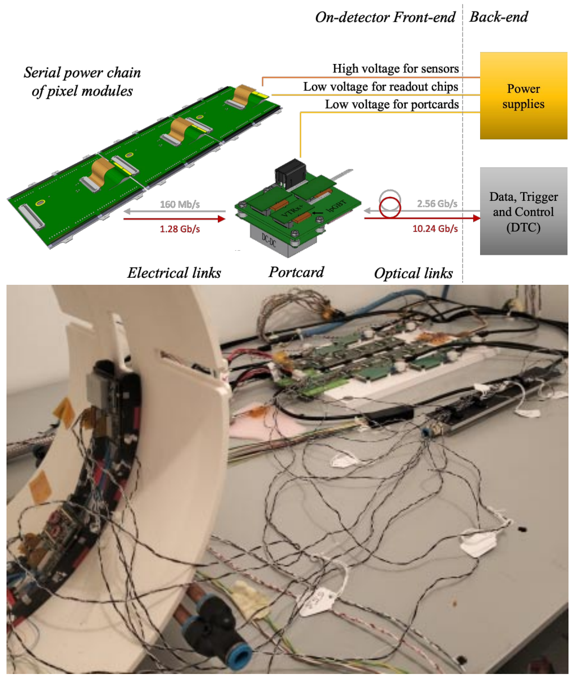

Fig. 4. – On the top a schematic view of the optical read-out. On the bottom is the implementation in the system test reading out six modules with the e-links connected to the portcards with the fiber in output.

without observing significant differences. The results of the calibrations at -31°C of the 8 modules powered in series are shown in fig. 3, with the noise being below 90 electrons. The fraction of noisy or dead pixels that are masked is below 0.05%.

The communication was also investigated as a function of the power consumption ensuring stable communication even if the chain is powered with 7 Ampere; this value is close to 10% headroom of the shunt current, which is the minimum threshold to safely operate the serial powered chain.

3. – TBPX system test with optical read-out

A more realistic scenario to emulate the future IT is the implementation of the final read-out, based on opto-electronics converter and fiber to the DTC. The optical read-out chain, shown in fig. 4, features the e-links, the portcards, and the octopus down to the back-end. The e-links are twisted pairs that connect electrically the modules to the LowPower GigaBit Transceiver, lpGBT, on the opto-electronics conversion board, the portcard. The portcard consists of several parts: a DC-DC converter and three lpGBT chips which are piloting three VTRx+. The DC-DC converter regulates the power for the different components. The VTRX+ are laser drivers that actually performs the optical conversion and send the signal through a fiber fan-out with up to 12 fiber links, the octopus. These fibers are connected to the DTC on FC7, a μTCA compatible card for generic CMS data acquisition, through a specific board.

In the system test this has been implemented with five 1.6 m e-links and 1 m e-links

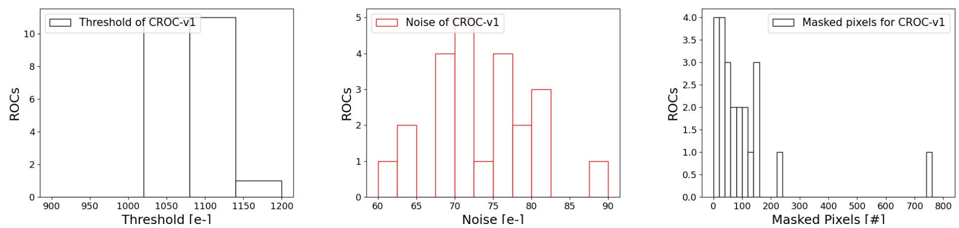

Fig. 5. – The results of the calibrations for the modules powered in series obtained with the optical read-out reading six modules only. Left are the thresholds, center is the noise of the tuned ROCs and right there is the number of masked pixels.

with four data lanes and one common command lane. In the final experiment the length of TBPX e-links will be 1.6 m, while the future e-links will have more data and command lanes each. Two portcards mounted on the mechanical prototype cartridge are used to read out the system test. The limited number of portcards forces the total number of modules that can be read-out at the same time, having only six of them optically read-out. A picture of the revised set-up after the optical read-out implementation is shown in fig. 4, with a close-up on the mechanical structure that hosts the portcards.

The communication with the optical read-out was assessed in first place, showing no issues even with the final read-out chain. Everything was tested in a wide temperature range showing no discrepancy at different temperatures. The modules were powered with 7.5 Ampere requiring $\sim$ 13.5 V at the power supply. The results of the calibration with the CO_2 temperature set to -27°C are shown in terms of threshold, noise and masked pixels in fig. 5.

The results confirm that there is no difference in between performing the tuning with the optical or the electrical read-out, having a noise below 90 electrons and the fraction of masked pixels below 0.05%. Also test of communication stability were performed observing similar performance between the two read-out chains.

The system is a close model of the final inner tracker, composed of the final mechanic prototype, the full-scale read-out chip and the entire read-out optical chain. Future updates will address the services, such as the multi service cable or the power supply prototype and the addition of modules equipped with sensors.

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