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Upgrade of the readout electronics for the ATLAS Liquid Argon Calorimeter(*)

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Summary. — The ATLAS Liquid Argon Calorimeter readout electronics will be upgraded for the HL-LHC. This includes the development of custom preamplifiers and shapers with low noise and excellent linearity, a new ADC chip with two gains and new calibration boards with excellent non-linearity and non-uniformity between all calorimeter channels. New ATCA compliant signal processing boards equipped with FPGAs and high-speed links receiving the detector data and performing energy and time reconstruction as well as a new timing and control system are also designed. Test results of the latest versions of the aforementioned components and the latest firmware development will be presented.

1. – Introduction

The current progress on the upgrade of the readout electronics for the ATLAS Liquid Argon (LAr) calorimeter in preparation for the High-Luminosity Large Hadron Collider (HL-LHC) era, expected to commence in 2029, is discussed.

The ATLAS Liquid Argon Calorimeter is designed to measure the energy and timing of photons, electrons, and hadrons produced by proton-proton collisions in the Large Hadron Collider (LHC), with sufficient sensitivity to detect minimum ionizing muons. It consists of a series of sampling calorimeters, encompassing a total of 182,468 readout cells that use liquid argon as the active material and absorbers made of lead, copper, or tungsten.

The LAr readout electronics system is divided into on-detector and off-detector components. The on-detector electronics shape and sample the signals from the cells at the LHC bunch crossing (BC) frequency of 40 MHz, transmitting a digitized pulse to the off-detector electronics. There, the pulse is processed to extract energy and time information for each cell, which is then sent to the trigger and data acquisition (DAQ) systems.

During the HL-LHC era, the ATLAS detector will experience an instantaneous luminosity of up to 7×10^{34} cm^{-2}s^{-1} (seven times the original LHC design), corresponding to approximately 200 simultaneous collisions per bunch crossing. In this high-luminosity

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environment, distinguishing signal from noise becomes more challenging, necessitating more granular shower information for the trigger system. Consequently, the ATLAS trigger system is being upgraded to a new architecture with a latency of 10 microseconds and a rate of 1 MHz at the hardware trigger level.

The LAr readout chain is required not only to accommodate the increased trigger rates but also because the current system will not withstand the full radiation dose of the HL-LHC. The planned design for the upgraded LAr readout is being developed, where cell data for each bunch crossing will be digitized and sent directly to the off-detector electronics, eliminating the need for an on-detector pipeline.

2. – LAr upgrade readout components

Figure 1 illustrates the architecture of the complete LAr calorimeter readout scheme for ATLAS in the HL-LHC era. The system specifications are driven by the experiment's physics goals. The readout electronics must accommodate a wide dynamic range of energy deposits: the lower end is defined by the energy deposited by minimum ionizing muons (MIP) in a single cell (50 MeV), while the upper end reaches approximately 3 TeV, which could result from electrons or photons produced in the decay of a new particle with a mass around 10 TeV. To ensure accurate measurements, the system must meet nonlinearity requirements of less than 0.1% for cell energies up to about 300 GeV. Additionally, all components must be capable of functioning under the full expected HL-LHC radiation dose, which corresponds to a total ionizing dose of 1400 Gy, including a safety factor of 1.5.

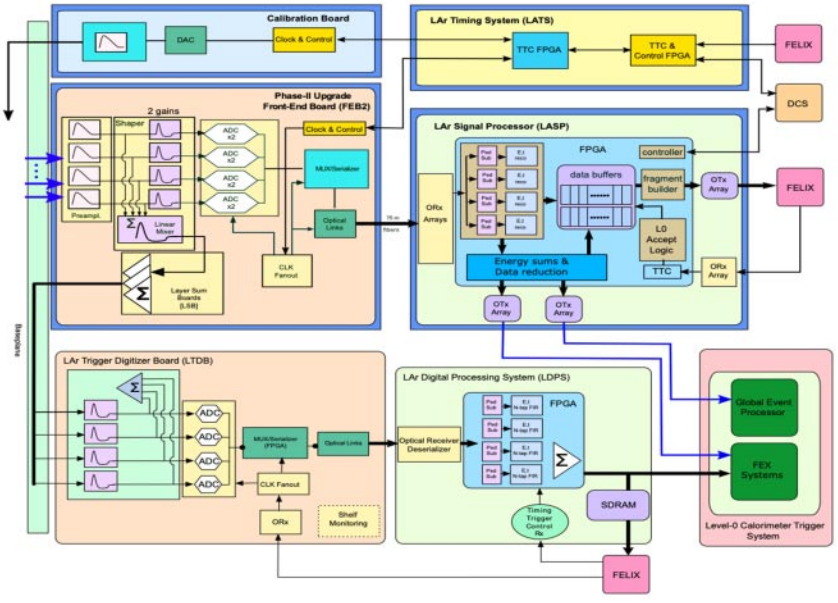

Fig. 1. – Layout of the LAr readout in the HL-LHC, including all on- and off-detector electronics. Calibration, Front-End and Signal Processing boards are under development for the Phase-II upgrades operation.

2˙1. *On-detector electronics.* – The on-detector LAr electronics includes second-generation front-end boards (FEB2) and calibration boards. Each FEB2 digitizes 128 channels, requiring a total of 1524 boards for the Phase-II upgrades. Each input line is capable of injecting signals into multiple cells simultaneously.

2˙1.1. Front-End board. The Front-End Board version 2 (FEB2) is designed to amplify and digitize signals for both trigger and energy reconstruction. It effectively manages the 16-bit dynamic range of calorimeters operating at 40 MHz, utilizing two gain scales. The digitized data is serialized and transmitted to the processing boards via the high-speed, radiation-hard lpGBT (Low Power Gigabit Transceiver) protocol developed at CERN. Each FEB2 digitizes 128 channels, requiring a total of 1524 boards for the Phase-II upgrades. A Layer Sum Board (LSB) is connected to the FEB2, providing analog trigger sums for digitization and processing.

The FEB2 features two custom-made ASICs: the pre-amplifier and shaper ALFE2, and the COLUTA V4 ADC. The ALFE chip, fabricated using 130 nm CMOS technology, has a 16-bit analog dynamic range. It performs CR-RC2 pulse shaping to convert the triangular ionization signal from the calorimeter into a bipolar pulse on two gain scales with a gain ratio of approximately 23. The latest version, ALFE v2, has met all specifications, including an Integral Non-Linearity (INL) of under 0.1% and an Equivalent Noise Current (ENI) of less than 350 nA for 10 mA channels and radiation hardness with 12 kGy dose.

Signals on the FEB2 are digitized by the COLUTA chip, an 8-channel, 15-bit, 40-MHz ADC fabricated using 65 nm CMOS technology with an MDAC-SAR architecture. Key specifications such as an Effective Number Of Bits (ENOB) above 11 and non-linearity below 0.1% have been achieved. Both ASICs are now in the pre-production stage following extensive testing, including irradiation tests.

2˙1.2. Slice test board. Earlier versions of the ALFE and COLUTA chips were integrated into a "slice-test board" to demonstrate functionality for 32 channels (instead of the 128 channels that will be the actual input to the FEB2). Alongside the ALFE and COLUTA, the slice-test board also included lpGBTs and VTRX+ modules, which are used for data transmission and control. The slice-test board successfully showcased the full digital functionality of configuring all the onboard chips. It also demonstrated the redundancy of bidirectional clock and control links, as well as the functionality for slow control and monitoring. The board's ability to reconstruct signals was tested by reading out LAr pulses of various amplitudes. Energy resolution, σ_E/E, for the highest energy pulses was found to be well below the specification of 0.25%. Tests are underway on a board fully populated with radiation-resistant solutions developed by CERN using bPOL48V and bPOL12V.

2˙1.3. Calibration board. Two custom ASIC chips, CLAROC and LADOC, will be utilized in the calibration board to inject physics-like pulses for the readout electronics calibration. CLAROC, fabricated using HV SOI CMOS XFAB 180 nm technology, functions as a high-frequency switch that generates pulses closely resembling the output of the LAr detector. The LADOC chip, produced with TSMC 130 nm technology, controls the current and a digital-to-analog converter (DAC) to produce precise pulse heights for calibration. Both chips must maintain stability under the same irradiation levels as the FEB2 chips.

The latest versions, CLAROC v4 and LADOC v2, have successfully met linearity specifications (less then 0.1% up to 300 Gev). The final LADOCv2b chip is in production

while CLAROCv4b is in submission for approval. In addition, the second prototype of the CABANEv2 calibration board is in production.

2˙2. *Off-detector electronics*. – The off-detector electronics consists of 30 LAr Timing System (LATS) boards and 278 LAr Signal Processor (LASP) boards. The LASP is responsible for digital signal processing and transmitting output data to the Trigger and Data Acquisition system. The LATS provides the Timing, Trigger, and Control (TTC) interface to the on-detector electronics. These off-detector electronics will be located in the counting room of the ATLAS experiment, shielded from collision radiation. Data transmission between the on-detector and off-detector electronics will primarily utilize the lpGBT protocol.

2˙2.1. LAr Timing System. The LATS distributes the Timing, Trigger, and Control (TTC) signals to the FEB2 and calibration boards and manages configuration and monitoring. A specialized ATCA board, known as the LATOURNETT, has been developed for this purpose and can control up to 72 boards simultaneously. It features a matrix of 12 Intel Cyclone 10 FPGAs for transmitting and receiving control and monitoring signals, along with another Intel Cyclone 10 FPGA for centralized control. The first prototype of this board is ready and passed test on FPGA firmware and infrastructure of the system. Prototype fabrication will begin in September 2024, and then the test campaign will begin including the integration of the system.

2˙2.2. LAr Signal Processor. The LASP receives data from the FEB2 and applies digital filtering algorithms to calculate the energy and time of the pulses. Each LASP blade will receive data from six FEB2s and will be equipped with two onboard Intel Agilex I-Series FPGAs, an Intel MAX10 FPGA, and a CERN IPMC, the latter two being used for board monitoring and control. Processed data from the LASP are sent to the Trigger and DAQ systems. Accompanying the LASP is a Smart Rear Transition Module (SRTM), which handles some of the high-speed serialization and encoding tasks and also performs monitoring and control functions. The SRTM fits into the backplane of the ATCA crate, with the LASP blade installed on the front side. a Test Board is in continuous operation due to the regular monitoring of temperature, voltage and current while the power supply, I2C sensors and FPGA configuration were validated. Firmware development and finalization of the LASP prototype are underway.

3. – Conclusion

The luminosity upgrade of the LHC necessitates the development of a new readout chain for the LAr calorimeter at the ATLAS experiment to meet the requirements of both the TDAQ system and radiation tolerance. Custom radiation-hard ASICs have been designed and tested. Using the slice-test FEB2 board, the interaction between the on-detector components was successfully validated. All electronic components will be replaced by 2029 and are designed to function throughout the lifetime of HL-LHC ($\sim$ 2041). All of the custom ASICs have passed the specifications and have entered the production phase. The design of the first prototype of the LASP board is at an advanced stage (including the firmware).

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