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Preliminary results on monolithic CMOS sensors with gain layer in 110 nm technology for the ALICE 3 experiment(*)

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Summary. — Monolithic Active Pixel Sensors (MAPS) benefit from a cost-effective implementation as they make use of commercial CMOS process, avoiding expensive interconnections to additional front-end ASIC. The ARCADIA collaboration has developed Fully-Depleted MAPS exploiting backside bias voltage to fully deplete the sensor, thereby enhancing charge collection efficiency and timing performance. Recent advancements have explored the introduction of a gain layer in MAPS to design a first monolithic LGAD prototype targeting 20 ps time resolution. The signal multiplication results in a higher signal-to-noise ratio and improved time resolution. This work illustrates preliminary characterization results of monolithic LGAD prototypes with an additional gain layer, based on a 110 nm CMOS technology developed in collaboration with LFoundry for the third run of the ARCADIA project.

1. – Introduction

ALICE 3 is a next-generation heavy-ion experiment proposed to be installed as a follow-up to the present ALICE experiment at CERN LHC [1] in Runs 5 and 6 of LHC, scheduled from 2035. The goal of such upgrade is to improve the data taking capability with respect to the present experimental apparatus, reaching 24 MHz in proton–proton (pp) collisions and 100 kHz in Pb–Pb collisions, by using an all silicon tracker complemented by a complete particle identification (PID) system, consisting of the Time Of Flight (TOF), the Ring Imaging Cherenkov detector (RICH), the Muon Identifier, and the Electromagnetic Calorimeter (ECal). In particular, the TOF targets a time resolution of 20 ps and it will cover a total area of 45 m^2, consisting of an inner and an outer

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TOF barrels and forward disks. Monolithic LGADs implemented in a standard CMOS process are among the technologies taken into account for this detector. Indeed, they represent a viable alternative to hybrid detectors, thanks to their reduced production costs and the undemanding manufacturing process.

2. – CMOS sensors with gain layer

Fully Depleted Monolithic Active Pixel Sensors (FD-MAPS) represent a state-of-the-art detector technology, as they have the advantage of collecting charges only by drift, ensuring a uniform and fast response over the pixel matrix. To further improve the time resolution, a gain layer implant was added underneath the collection electrode [2] in the FD-MAPS technology developed by the ARCADIA Collaboration in a 110 nm CMOS process. A schematic cross-section of a typical pad sensor, developed within the ARCADIA project, is depicted in fig. 1 (left). This n-on-n sensor features large n-doped collection diode on the front side, generating a uniform weighting field, crucial for timing application. The drawback is a larger capacitance, which implies a decreased Signal-To-Noise-Ratio (SNR). The design includes a p^+ boron-doped electrode on the backside of the n-substrate, allowing the bias voltage to be applied from the backside (V_{back}), where the depletion begins. An additional highly n-doped epitaxial layer is located above the n-type substrate with the aim to increase the voltage required for the onset of punch-through [3]. In this configuration, CMOS readout electronics can be placed in the p-wells and n-wells adjacent to each sensor pad, shielded by deep p-wells. Figure 1 (right) illustrates a cross section of the designed monolithic sensor with the addition of a gain layer. Such layer generates a high-field region enabling charge multiplication by impact ionization, when a sufficiently high voltage is applied at the front-side. The introduction of the gain layer represents a promising solution to improve the SNR and, as a consequence, the sensor timing performance. Each sensor pad is AC-coupled to the preamplifier, since the voltage applied at the collection electrode (V_{top}) needed for the operation of the detector is typically much larger than the voltage delivered to the CMOS readout circuitry.

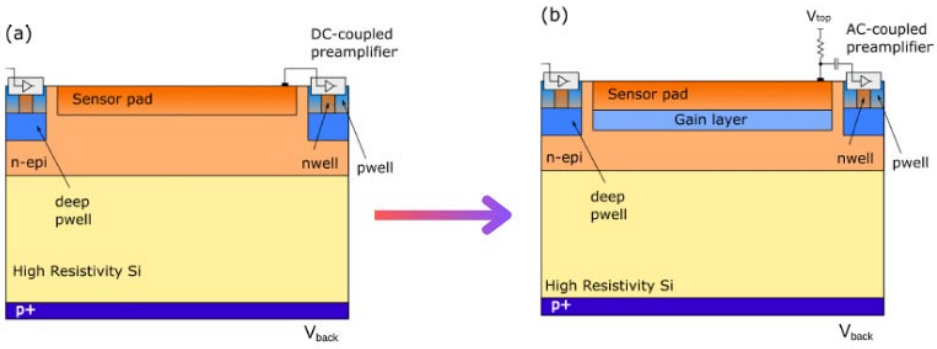

Fig. 1. – Schematic cross section of the ARCADIA pixel without gain, DC coupled (left) and an AC coupled pixel with gain (right). Picture from [2]

3. – TCAD and Monte Carlo simulations

The response of the ARCADIA CMOS sensors with gain layer was simulated using the Allpix^2 framework [4]. The simulation domain is represented by a single pixel with dimensions 250 μm $\times$ 140 μm and a thickness of 48 μm, starting from a 2D TCAD simulation of the pixel cross section (length and thickness of the pixel) and adding in Allpix^2 a fictitious third component for the width. A V_{top} voltage of 45 V and V_{back} voltage of -40 V were applied. The Allpix^2 framework combines TCAD-simulated electric fields with a GEANT 4 [5] simulation of the particle interaction with matter. The electric field map is shown in fig. 2 (left), where it is clearly visible the high electric field region on the top side, due to the presence of the gain layer. In particular, for each propagation step, the induced charge on the electrode n^+ is calculated via the Shockley-Ramo theorem as $Q_n^{ind} = \int_{t_0}^{t_1} I_n^{ind} dt = q(\psi(x_1) - \psi(x_0))$, where I_n^{ind} is the induced current on electrode n^+ and ψ is the function describing the weighting potential displayed in fig. 2 (right). The gain can be estimated as the ratio between the MPV of the Landau distribution of the collected charge with and without enabling the multiplication model. In this work the impact ionization coefficients follow the Okuto-Crowell model [6]. Figure 3 shows the collected charge distributions obtained simulating 10000 events in each configuration. Pions with an energy of 180 GeV were impinging randomly in a 100×100 μm^2 central area of the pixel. By comparing the MPVs, a gain of around 2 can be estimated, in agreement with the measurements [7].

3˙1. *Sensor layouts.* – To evaluate the effect of the pixel termination layout on the charge collection process, two different layouts, labeled as A1 and A2, have been designed [7] and are schematically represented in fig. 4. In the pixel with layout A1 there is no free space between the deep p-wells and the gain layer implant, while in the A2 layout a gap region, highlighted with red dashed circles, is preserved between them. In the A1 type, the charges generated at the pixel periphery are multiplied, as they are conveyed in the avalanche region because of an almost continuous p-type implant at the pixel borders. On the contrary, in the A2 layout, charges from the periphery are not multiplied because of the gap between the two p-type implants which causes the loss of the electrical continuity. For this reason, the layout A2 should be able to distinguish

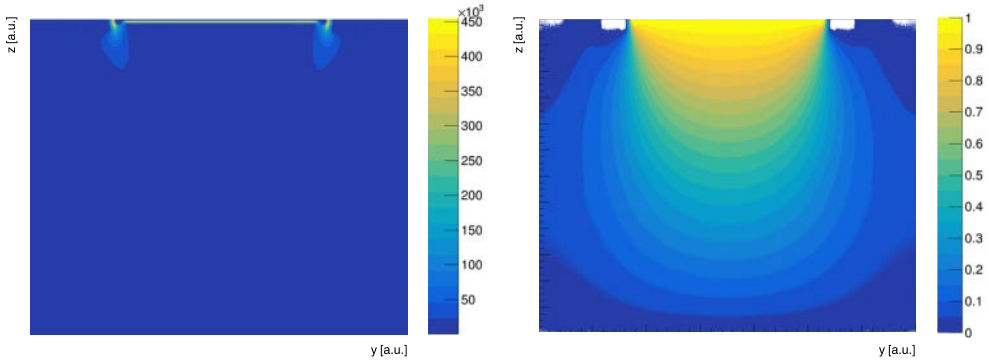

Fig. 2. – Electric field (left) and weighting potential (right) of a single pixel, extracted from Allpix^2. The y and z coordinates represent the side lengths and the thickness of the pixel, respectively.

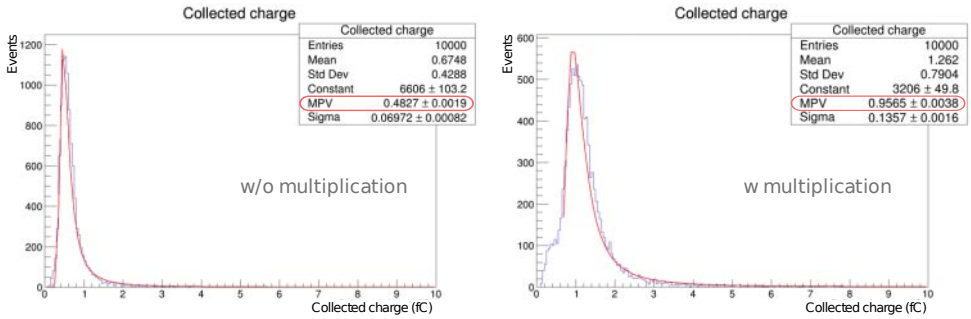

Fig. 3. – Collected charge distribution without (left) and with (right) multiplication model.

between multiplied and not multiplied signals, coming from the central or the edge area of the pixel, respectively, leading to a better time resolution due to the possibility of isolating the multiplied signals.

4. – Preliminary laboratory measurements

A preliminary characterization of the sensors has been performed in the laboratory. Figure 5 shows the current measured on the top electrode (left) and at the bottom one (right) by varying the voltage applied at the backside, for both the A1 and A2 layouts. In these measurements, the voltage applied at the top-side electrode was fixed at 35 V. The green box on the left plot indicates the region in which the sensors can be considered fully depleted, since a steep decrease in the top current is observed, meaning that the resistive path between the pixel and the guard ring has been closed. The difference in the behavior of the A1 and A2 structures can be attributed to their different layout, as the presence of the gap in the A2 shifts the depletion point to higher V_{back}. From fig. 5 (right) it is possible to observe in which voltage range the punch-through phenomenon starts to play a role. It occurs when the voltage applied to the backside electrode rises above a certain value, causing a hole current to flow between the deep p-well, on the front side, and the p^+ doped electrode, at the bottom of the sensor. This current increases exponentially and sensor operation in condition of large punch-through current has to be avoided, as it can lead to an excessive power consumption.

5. – The Monolithic CMOS Avalanche Detector PIXelated

The Monolithic CMOS Avalanche Detector PIXelated (MadPix) is 16.4 × 4.4 mm^2 large chip composed by 8 matrices of pixels. Each matrix comprises 64 pixels divided in

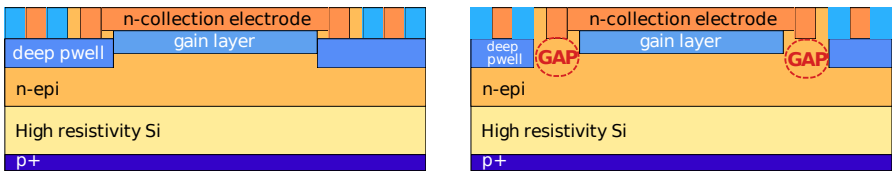

Fig. 4. – Schematic cross section of a pixel with layout A1 (left) and A2 (right).

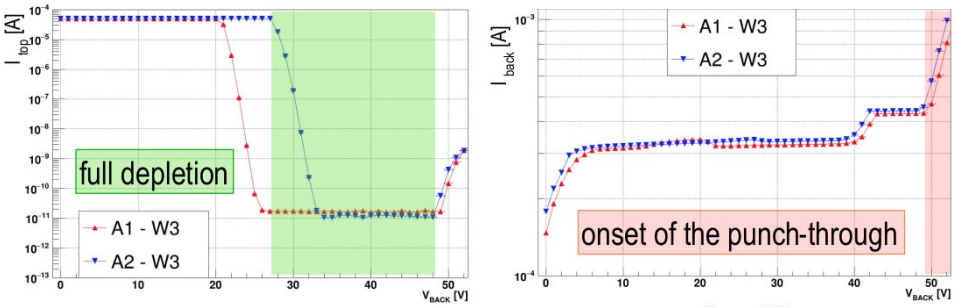

Fig. 5. – Current measured at the top electrode (left) and at the backside electrode (right) as a function of the voltage applied at the backside electrode for A1 and A2 layouts. The voltage applied at the collection electrode was fixed at 35V.

8 rows and 8 columns. The layout is shown in fig. 6. The pixel size is 100 × 250 μm^2, while the 1.2 V front-end electronics is placed in a 8 × 250 μm^2 p-well implemented in the long side dividing two adjacent pixels. In addition, 3.3 V source follower buffers are placed outside the matrices and inside the external guard ring. This one is polarized to a positive voltage below 10 V and surrounds each matrix preventing early breakdown phenomena at the borders. The four matrices differ for the layout terminations, as described in sect. **3**˙1 and for different layouts of the coupling capacitor.

5˙1. *In-beam measurements*. – A test beam campaign was carried out at the Proton Synchrotron at CERN with a beam composed by a mixture of protons and pions with a momentum of 10 GeV/c, to measure the time resolution of the MadPix chip. Two planes were used in the measurements: the Device-Under-Test (DUT) and a 1 × 1 mm^2 LGAD [8] with a thickness of 35 μm, employed as trigger plane. In this work, the time resolution of MadPix has been estimated from the crossing time distributions obtained by applying a threshold at a constant fraction of the total signal amplitude. The results for the measured time resolution as a function of the applied threshold are shown in fig. 7 for the A2 layout at two different top voltages V_{top}. An improvement in the timing performance is observed when the V_{top} is increased to 45 V. When V_{top} is set to 30 V, the multiplication mechanism is significantly reduced, resulting in a lower signal amplitude compared to the 45 V configuration. Notably, the time resolution worsens near the minimum and maximum thresholds because in that regions the signal has a lower slope, translating into a higher jitter component and this effect is more pronounced in the 30 V configuration. On the other hand, for V_{top} = 45 V, the slope of the signal remains constant over a wider range of applied thresholds, resulting in more stable timing performance. The analysis procedure is presented in detail in [9], where a different

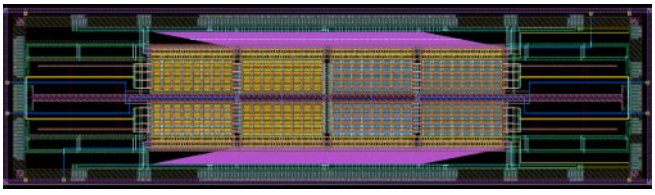

Fig. 6. – Monolithic CMOS Avalanche Detector PIXelated (MadPix) layout.

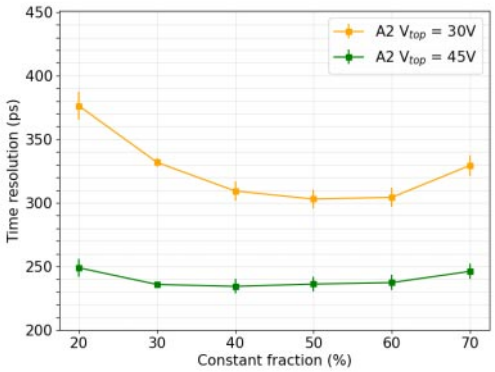

Fig. 7. – Time resolution as a function of the constant fraction threshold.

approach was followed, yet similar results were obtained. The reason for the measured time resolution, about 230 ps for $V_{top} = 45$ V, still far from the TOF requirements, has been deeply investigated and understood through a numerical study based on TCAD simulations [9], confirming an error during the fabrication process. Indeed, the energy of the ion implantation was set to a value 30% lower than the expected one, causing a shallow gain layer.

6. – Conclusions

A first monolithic LGAD prototype implemented as MAPS with gain layer in a 110 nm CMOS process has been produced and characterized in laboratory and in a test beam. The time resolution was estimated to be below 250 ps in the best case from in beam measurements. Both measurements and simulations confirmed a sensor gain of ∼2, lower than the expected one. A new short-loop run has been submitted and it should allow to reach the desired gain $G \sim$ 10-30.

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